

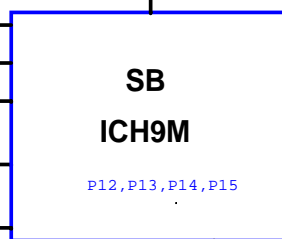
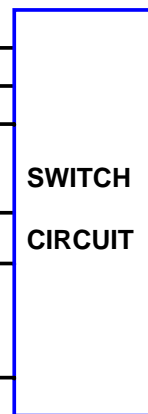
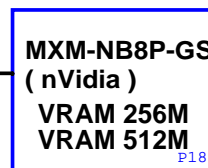
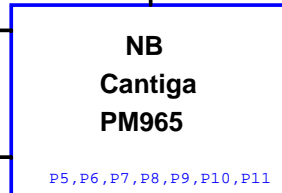
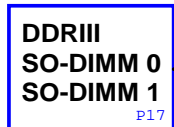
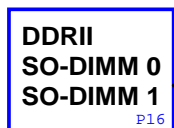
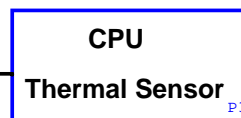
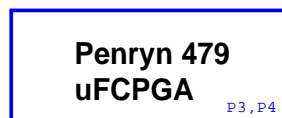
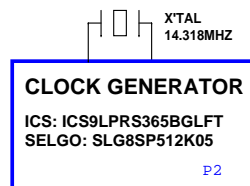
ZY2 SYSTEM BLOCK DIAGRAM

BOM MARK

E@ EXT VGA 要打
268@ AUDIO 268 要打
D@ DOCK
D2@ DDR2 要打
SP@ 特殊(EXT VGA OR DDR2)
LC@ LOW COST 要打
ED2@ EXT VGA & DDR2 要打
CB@ CARDBUS 要打
NSF@ Non ASF 要打

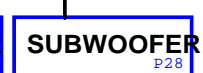
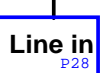
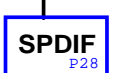
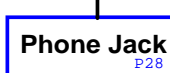
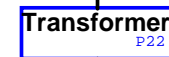
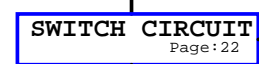
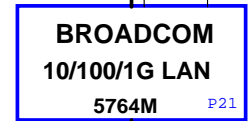
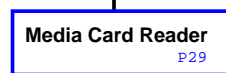
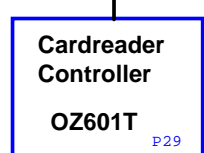
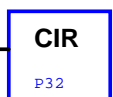
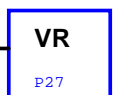
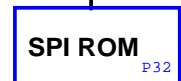
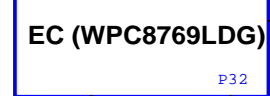
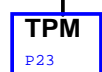
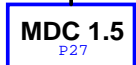
I@ INT VGA 要打
888@ AUDIO 888 要打
D3@ DDR3 要打
ND@ NON DOCK 要打
NLC@ NON LOW COST 要打
TPM@ INT TPM
ID2@ INT VGA & DDR2 要打
ED3@ EXT VGA & DDR3 要打
ID3@ INT VGA & DDR3 要打
ASF@ ASF 要打
NCB@ NON CARDBUS 要打

LOW COST
1. MINI CARD 1 SLOT
2. NON DOCK
3. NON CARDBUS
4. NON ASF
5. NON HDMI

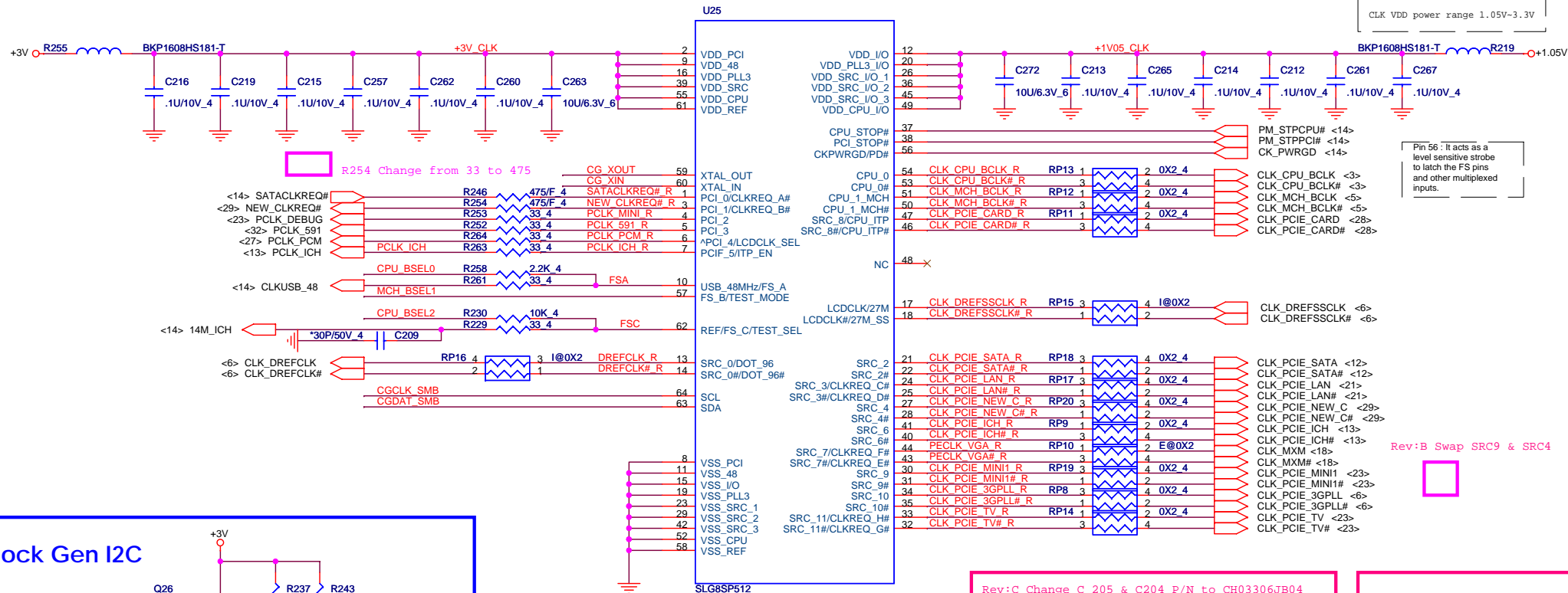


PCI-Express

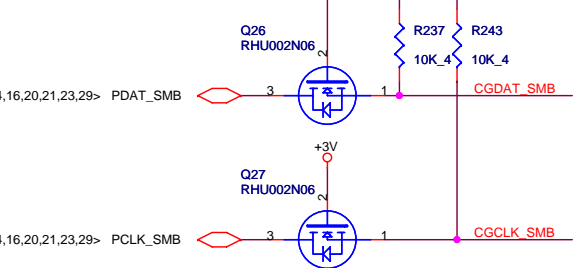
PCI-E-1



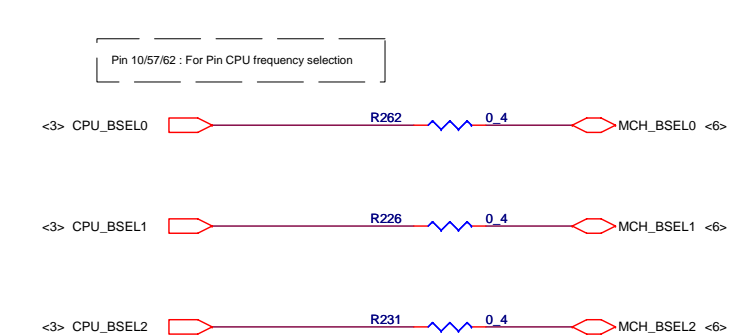
Clock Generator



Clock Gen I2C



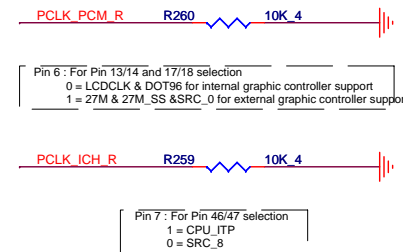
CPU Clock select



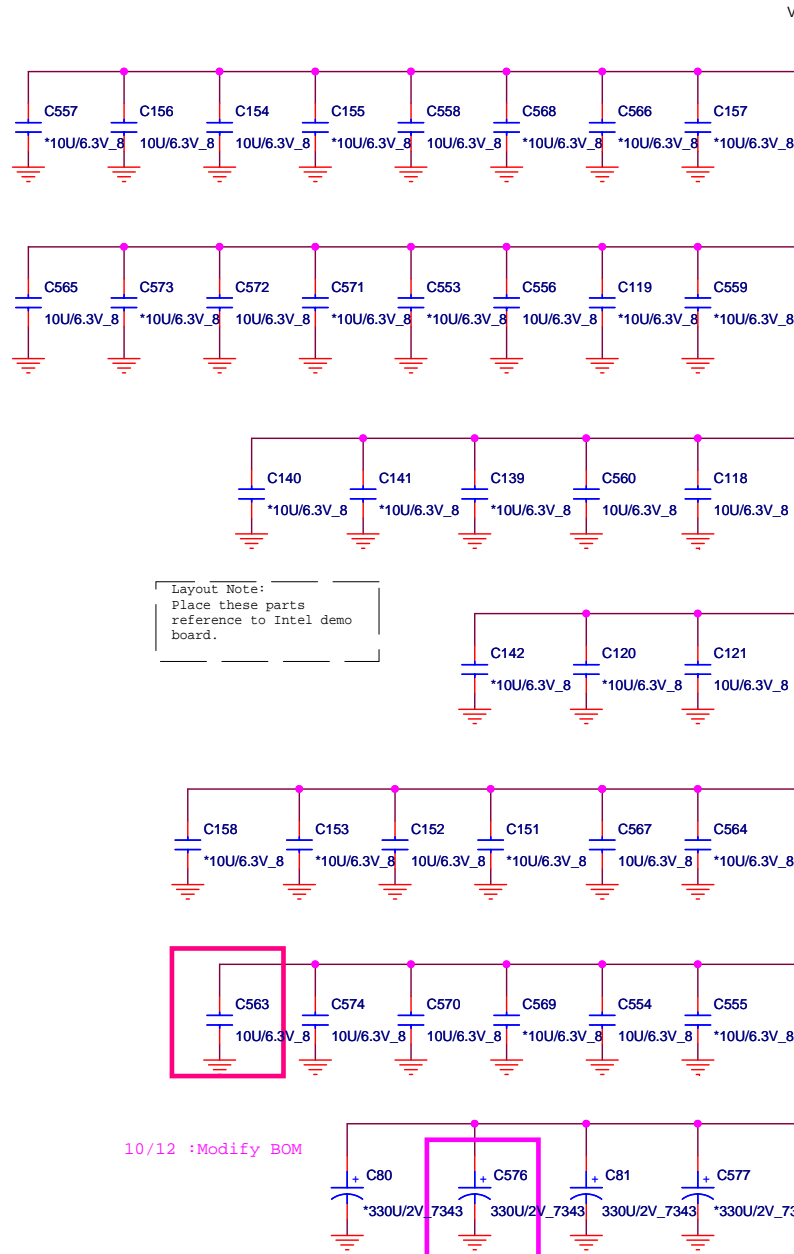
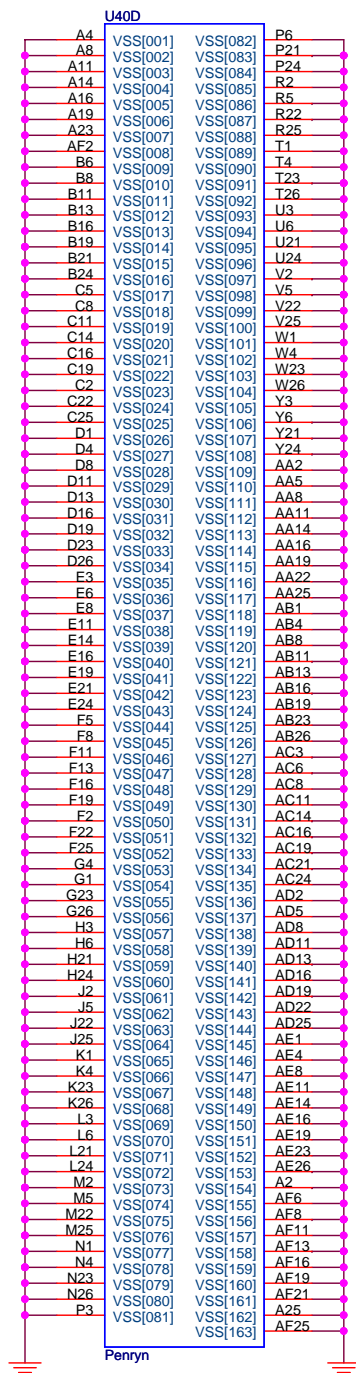
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table



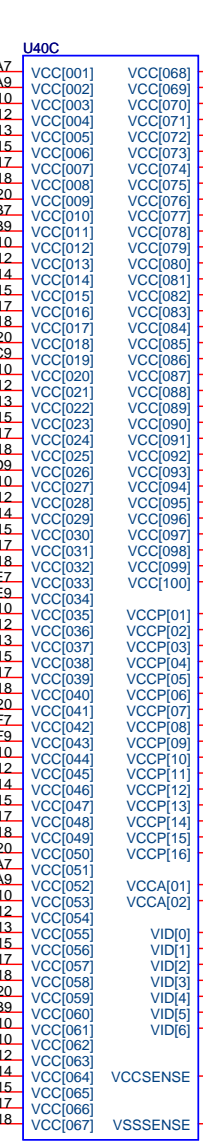
Quanta Computer Inc.
PROJECT : ZY2 & ZY6



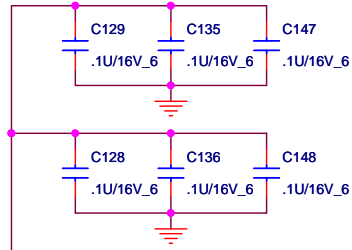
Layout Note:
Place these parts
reference to Intel demo
board.

10/12 :Modify BOM

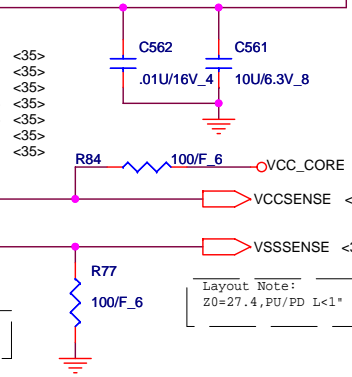
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2



Layout Note:
Inside CPU center cavity in 2 rows



Layout Note:
VCCA CAP close to Pin
VCCA : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)



VCCA : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)

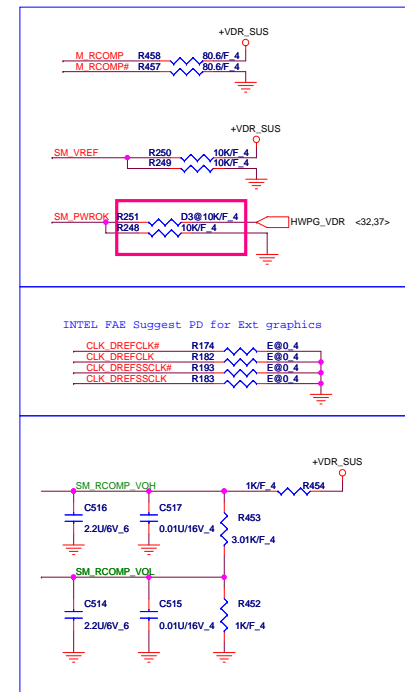
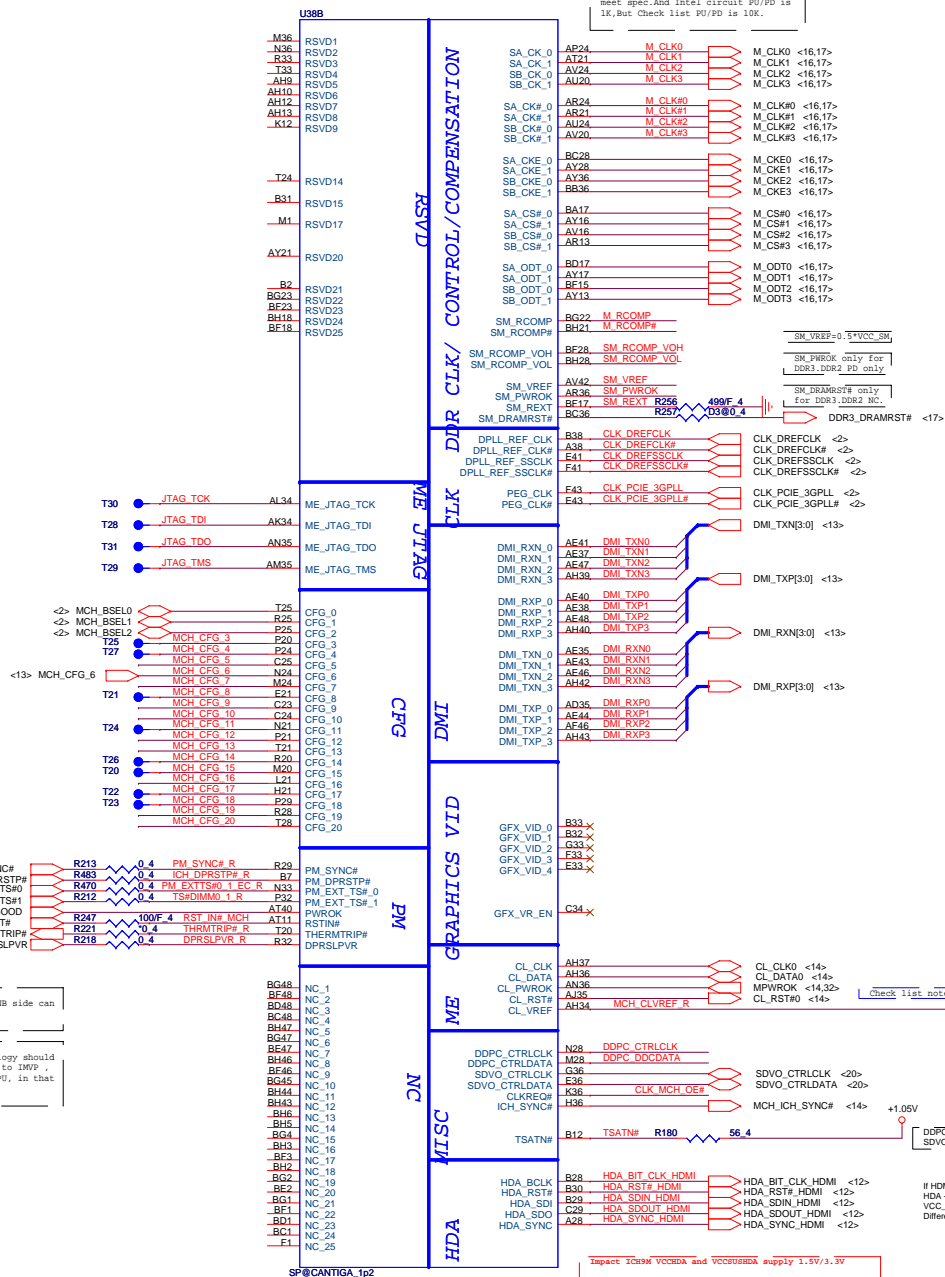
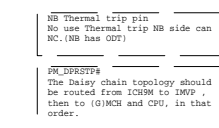
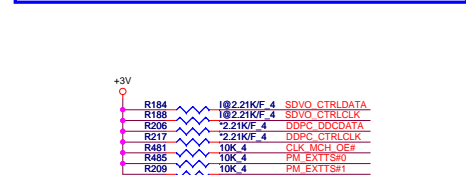
Layout Note:
Z0=27.4, PU/PD L<1"



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev 1A
	CPU Power	
Date:	Tuesday, April 08, 2008	Sheet 4 of 40

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	WE TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present



1.05V

R224
1KF_4

V

R233
511/F_4

10V_4


Pin C
Pin B

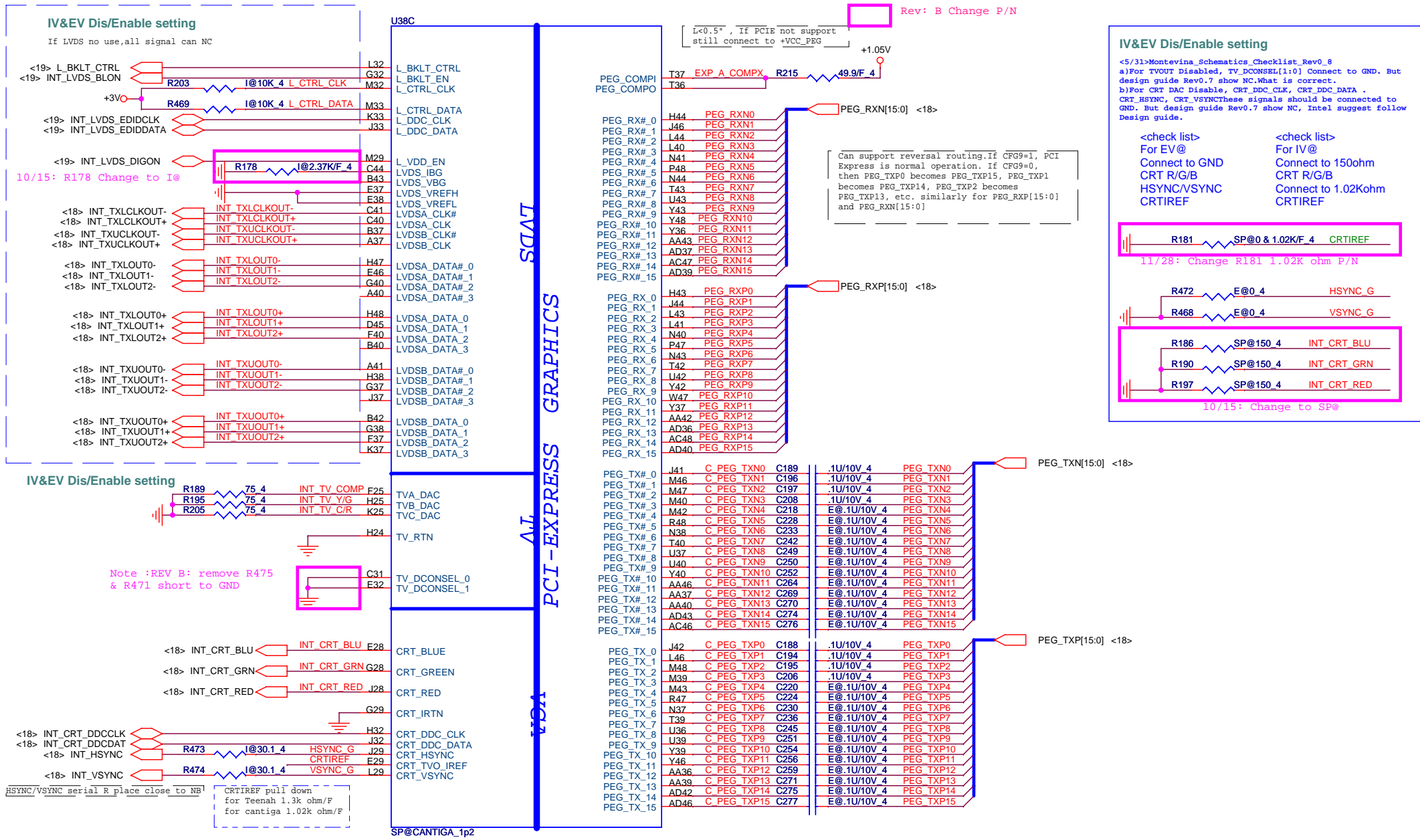
-> Checklist ver0.8>
 If TSATN# is not used, then it must be terminated
 with a 56-Ohm pull-up resistor to VCCP.

<> Pin odd check issue>
 Canliga EDS 0.7 change Ball B12 to TSATN# from SATN

Impact ICH9M VCCBDA and VCCSUSBDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for IHDMT, VCCBDA and VCCSUSBDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

 Quanta Computer Inc. PROJECT : ZY2 & ZY6		
Size	Document Number GMCH DMI	Rev 1A
Date:	Tuesday, April 08, 2008	Sheet 6 of 40



IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0.8

a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC. What is correct.

b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC these signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>
For EV@
Connect to GND
CRT R/G/B
HSYNC/VSYNC
CRTIREF

<check list>
For IV@
Connect to 150ohm
CRT R/G/B
Connect to 1.02Kohm
CRTIREF

R181 SP@0 & 1.02K/F 4 CRTIREF

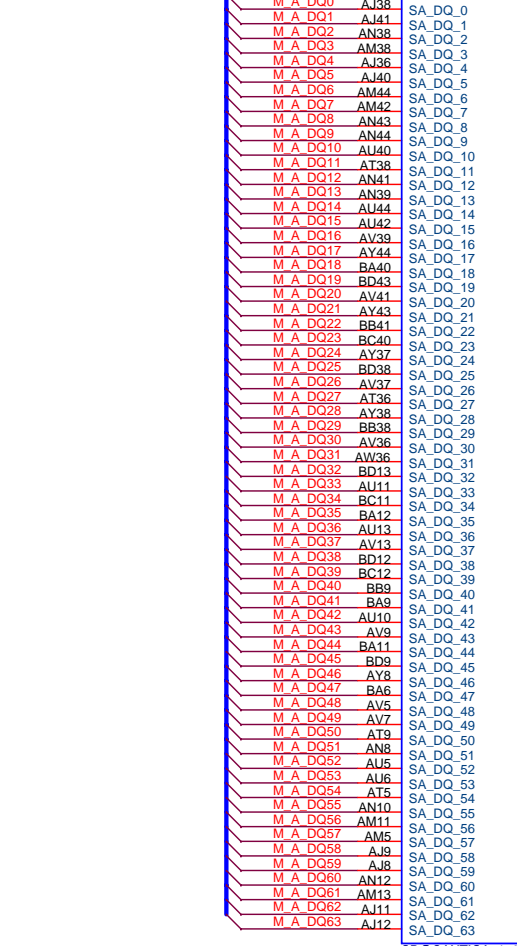
11/28: Change R181 1.02K ohm P/N

R472 E@0.4 HSYNC_G
R468 E@0.4 VSYNC_G

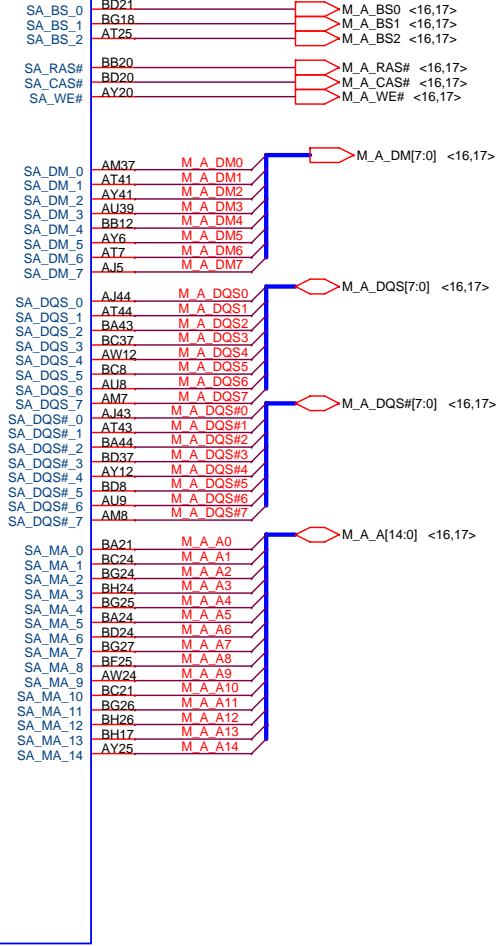
R186 SP@150_4 INT_CRT_BLU
R190 SP@150_4 INT_CRT_GRN
R197 SP@150_4 INT_CRT_RED

10/15: Change to SP@

<16,17> M_A_DQ[63:0]

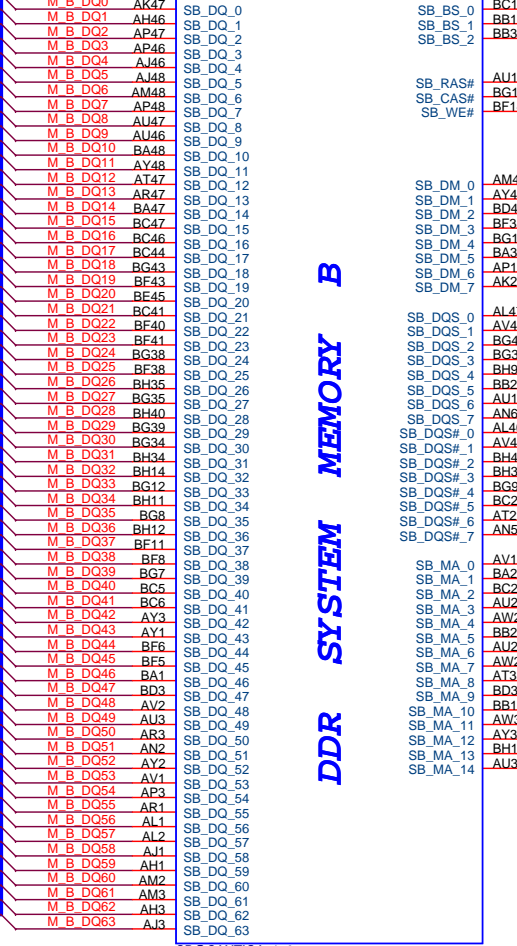


DDR SYSTEM MEMORY A

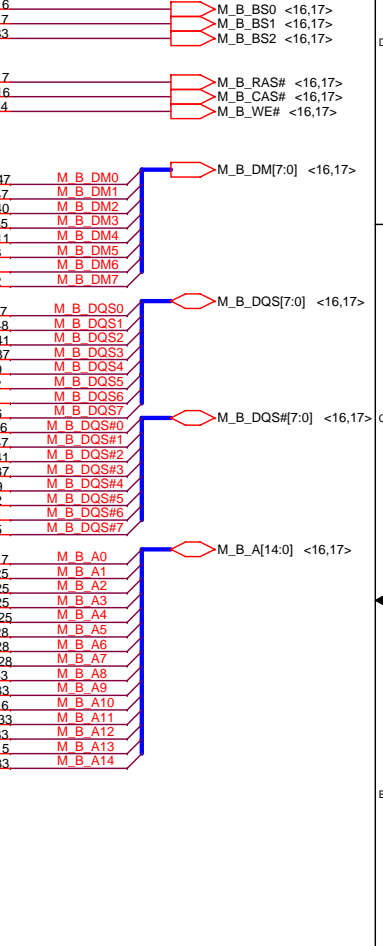


SP@CANTIGA_1p2


<16,17> M_B_DQ[63:0]



DDR SYSTEM MEMORY B



SP@CANTIGA_1p2



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

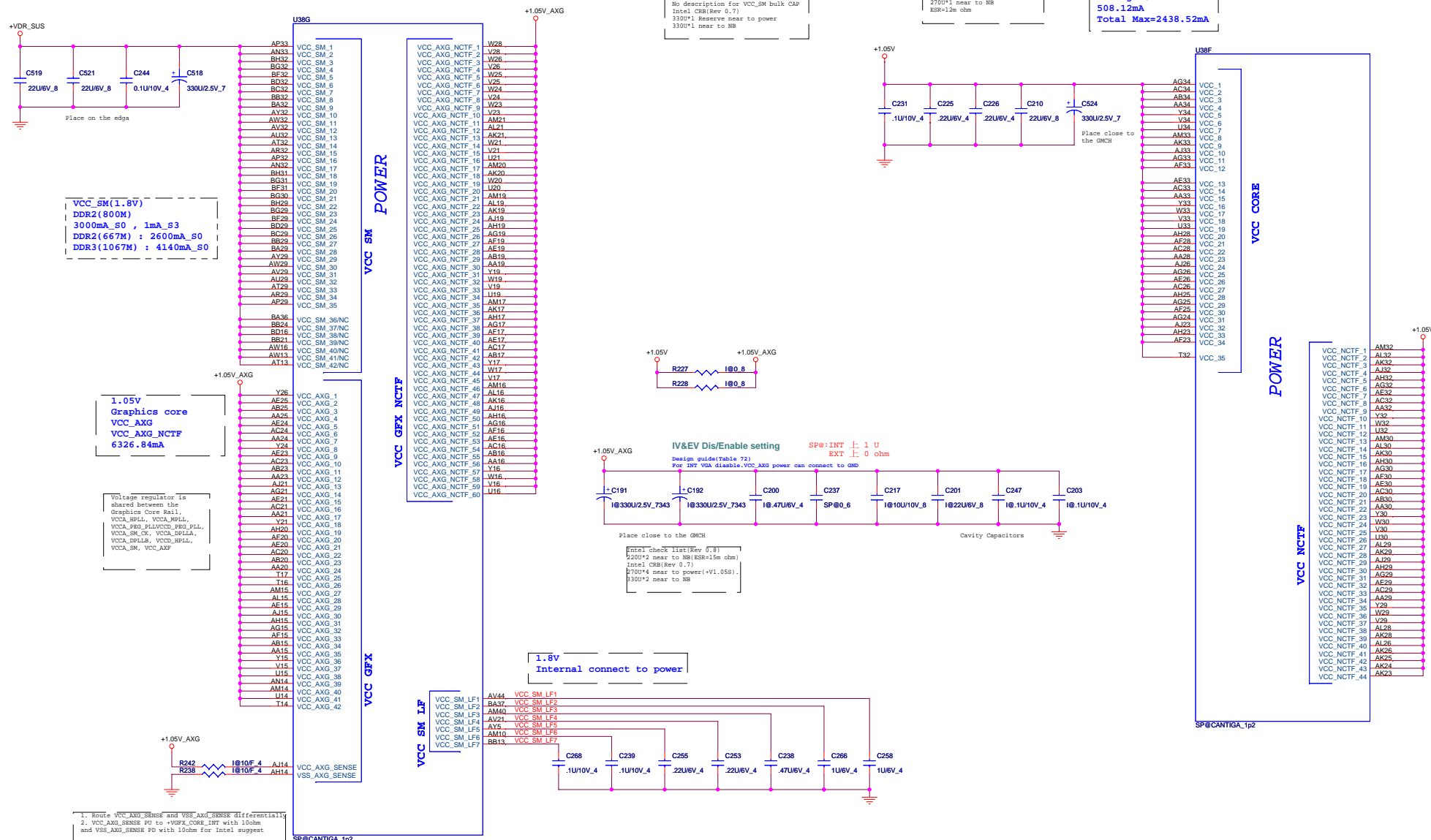
Size	Document Number	Rev
	GMCH DDRII	1A
Date:	Tuesday, April 08, 2008	Sheet 8 of 40

GM	TDP	10.5~12W
GS	TDP	7~8W
PM	TDP	7W

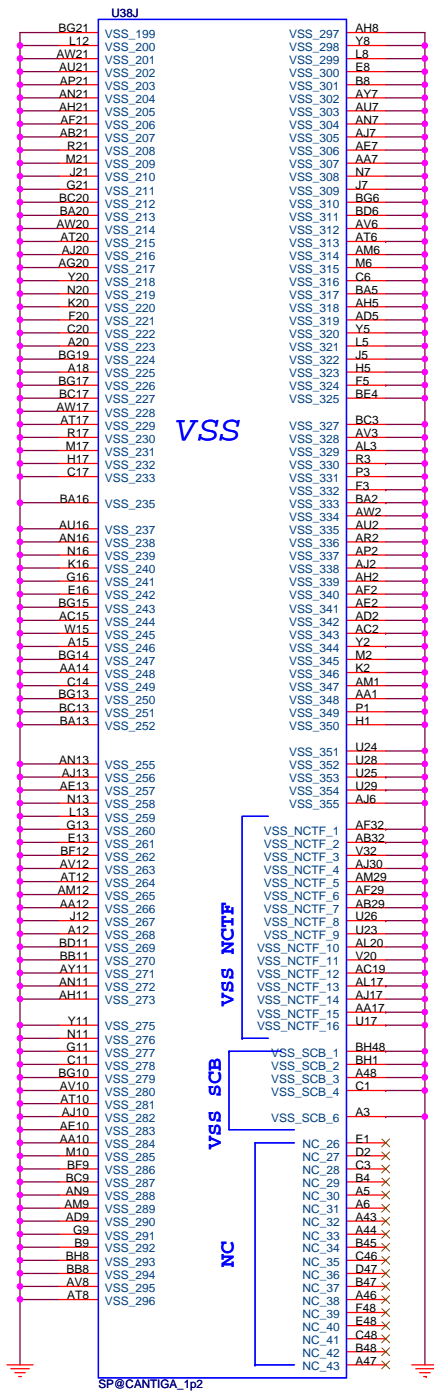
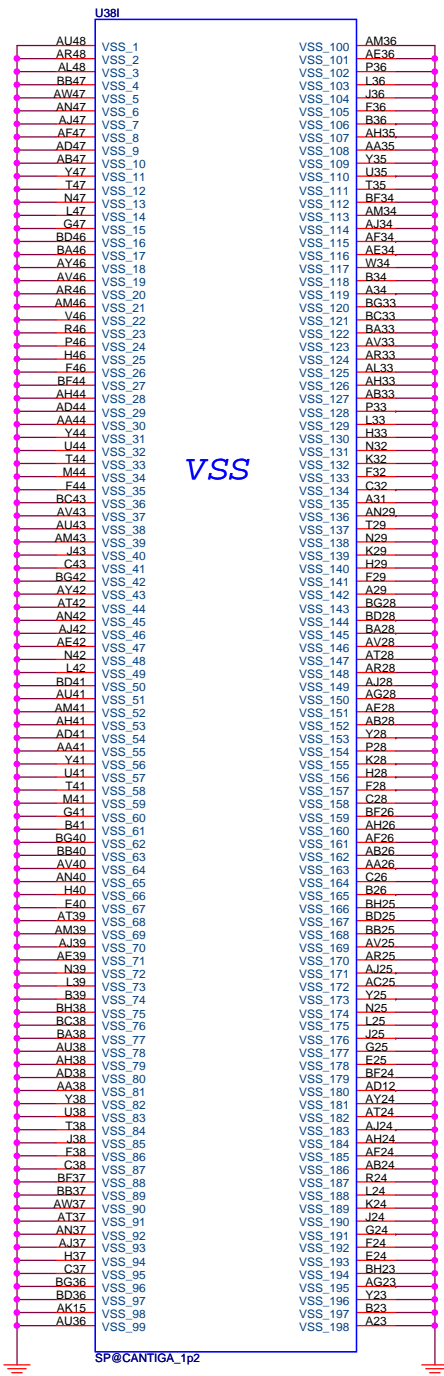
```
Intel check list(Rev 0.8)
No description for VCC_SM b
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
```

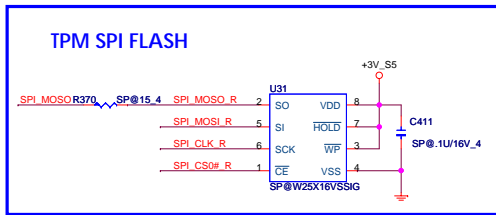
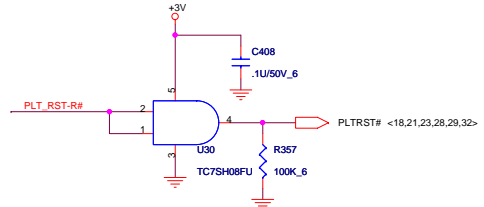
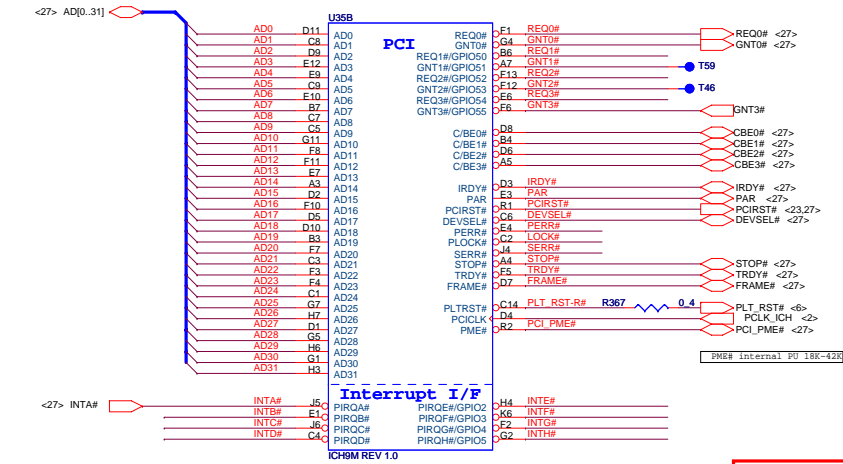
```
Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm
```

```
VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA
```



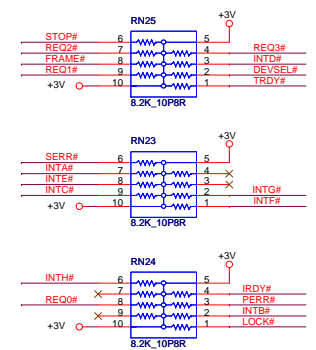
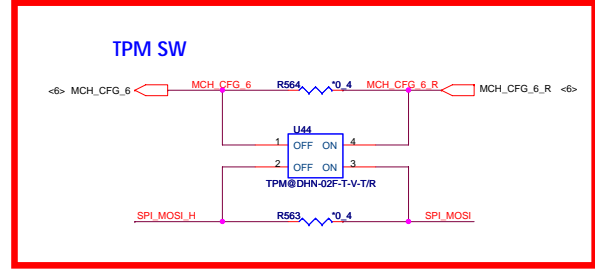
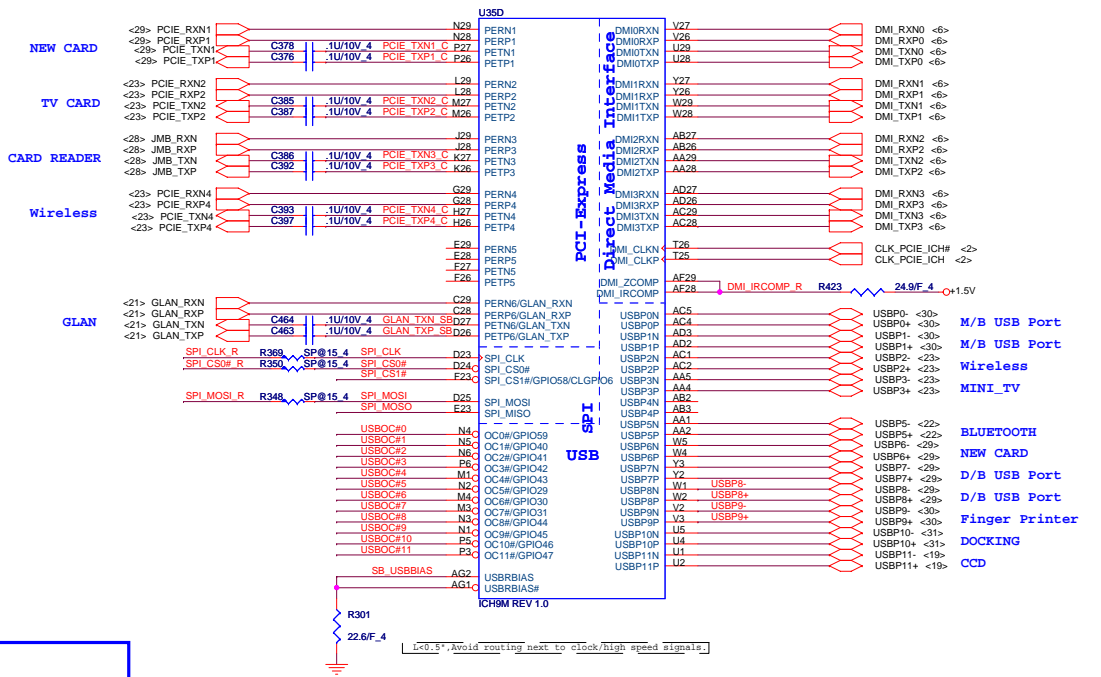






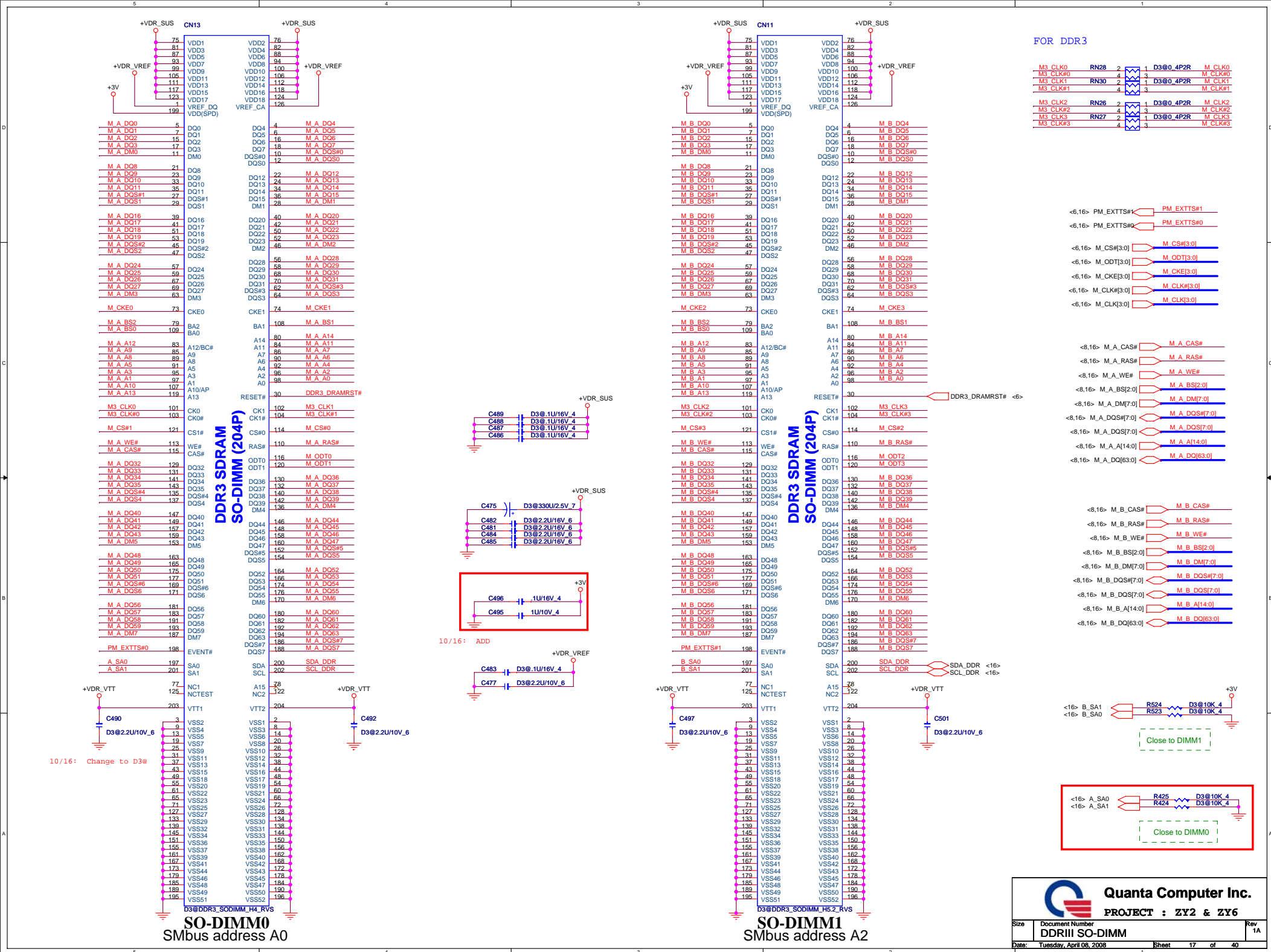
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD		
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI(Default)	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC	



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTA#	OZ601T

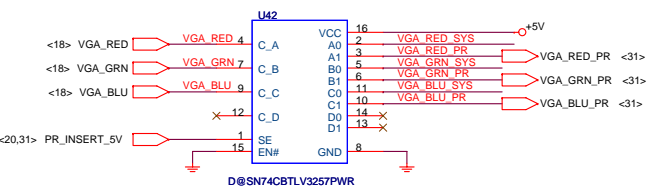




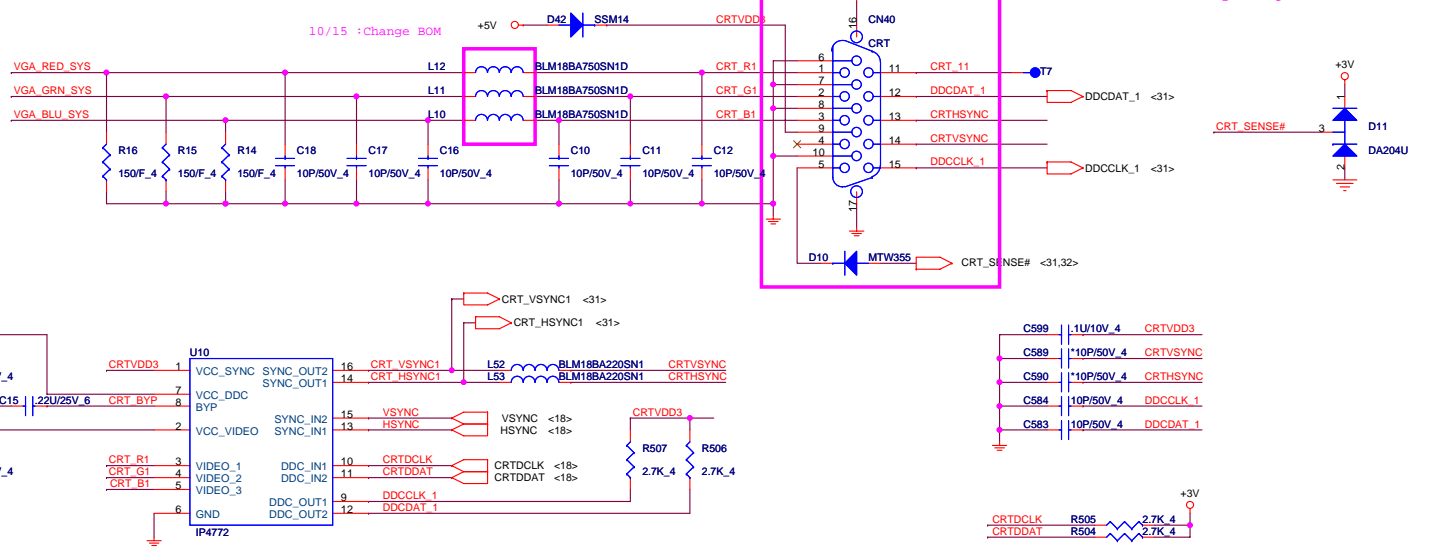


CRT Select

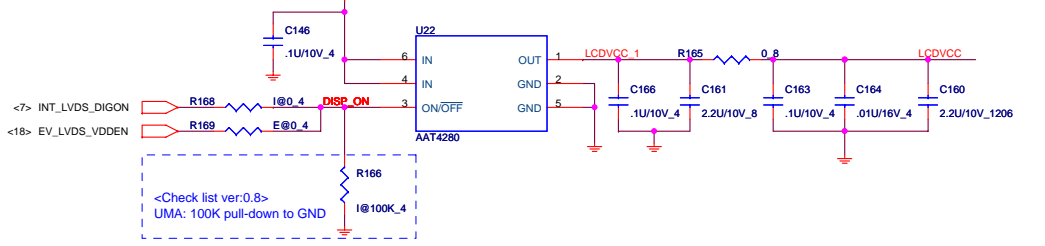
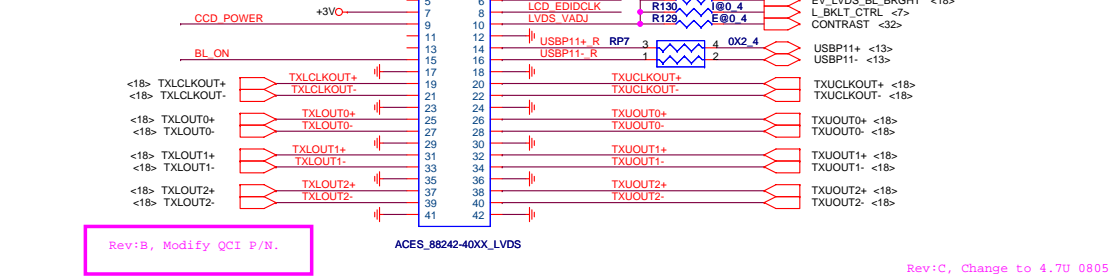
CRT SWITCH



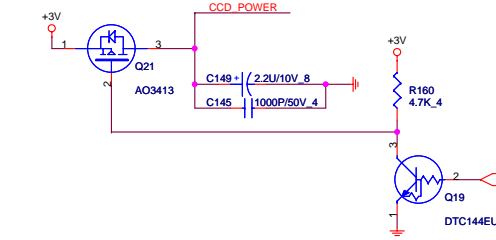
CRT CONNECTOR AND ESD



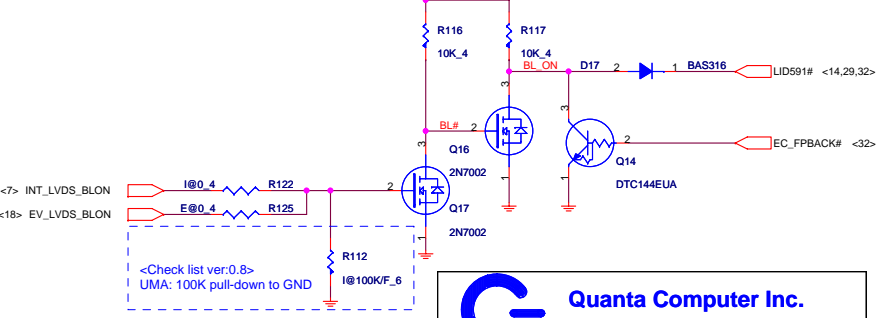
LVDS



CAMERA MODULE CONNECTOR

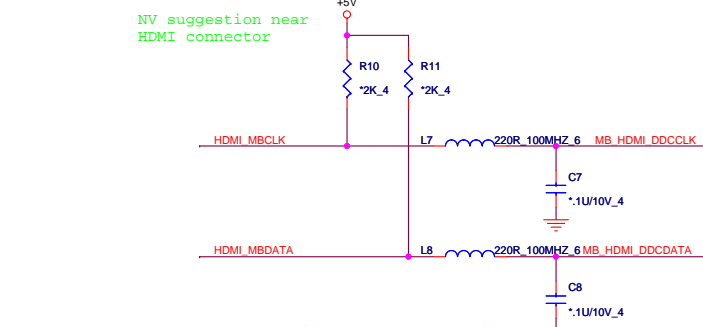
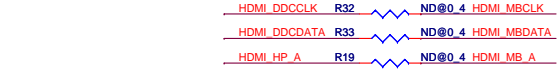
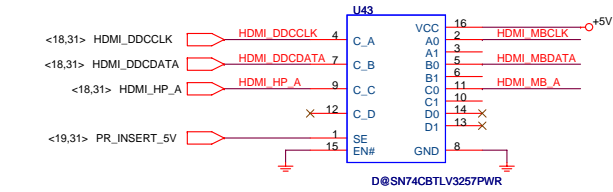
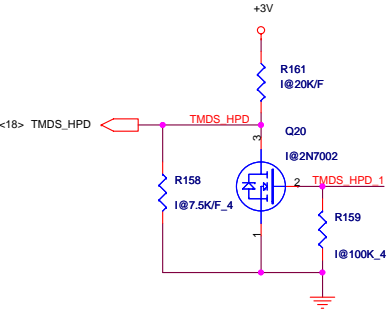


Backlight Control

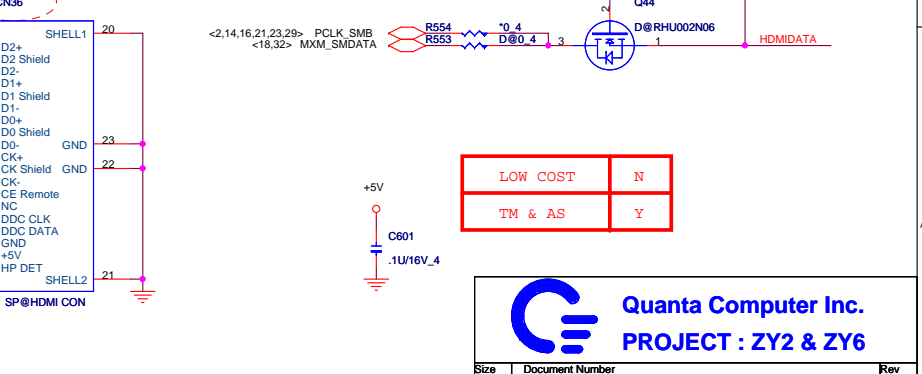
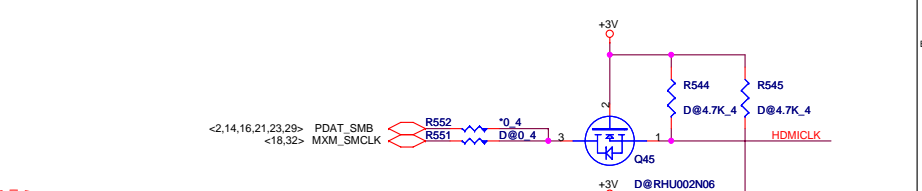
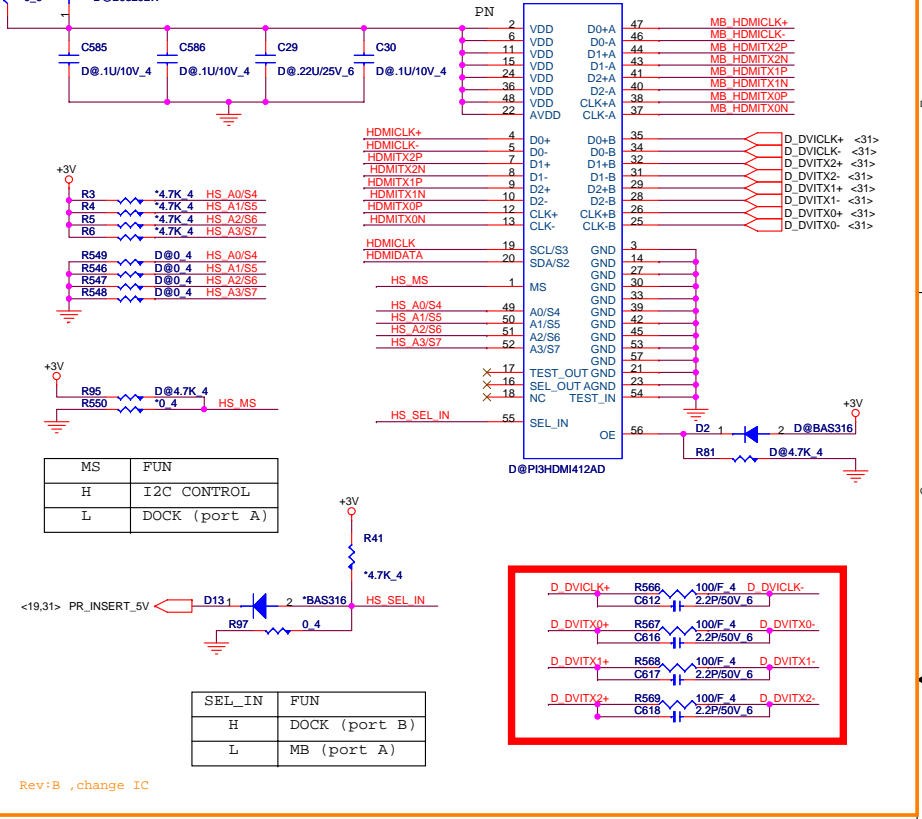
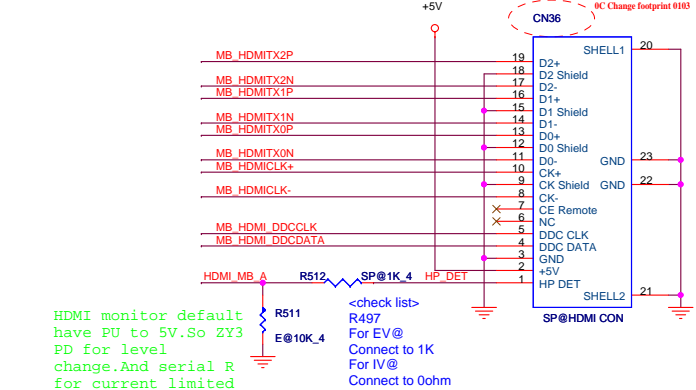
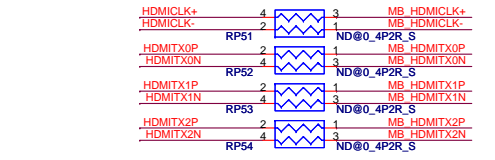
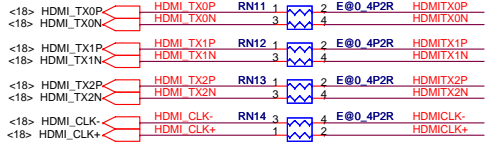
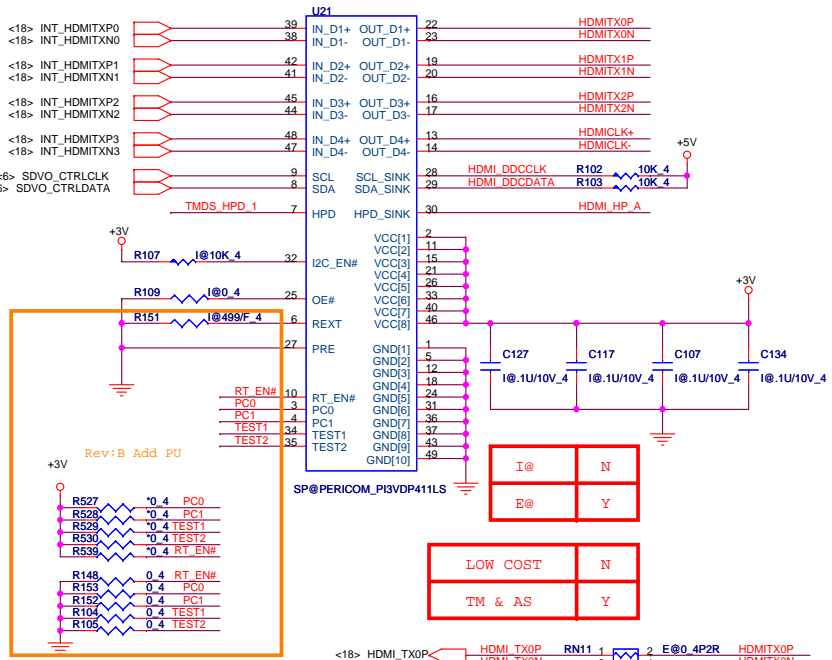



DVI-I CONNECTOR (DVI-D)

	QCI P/N
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	



WWW.AliSaler.Com

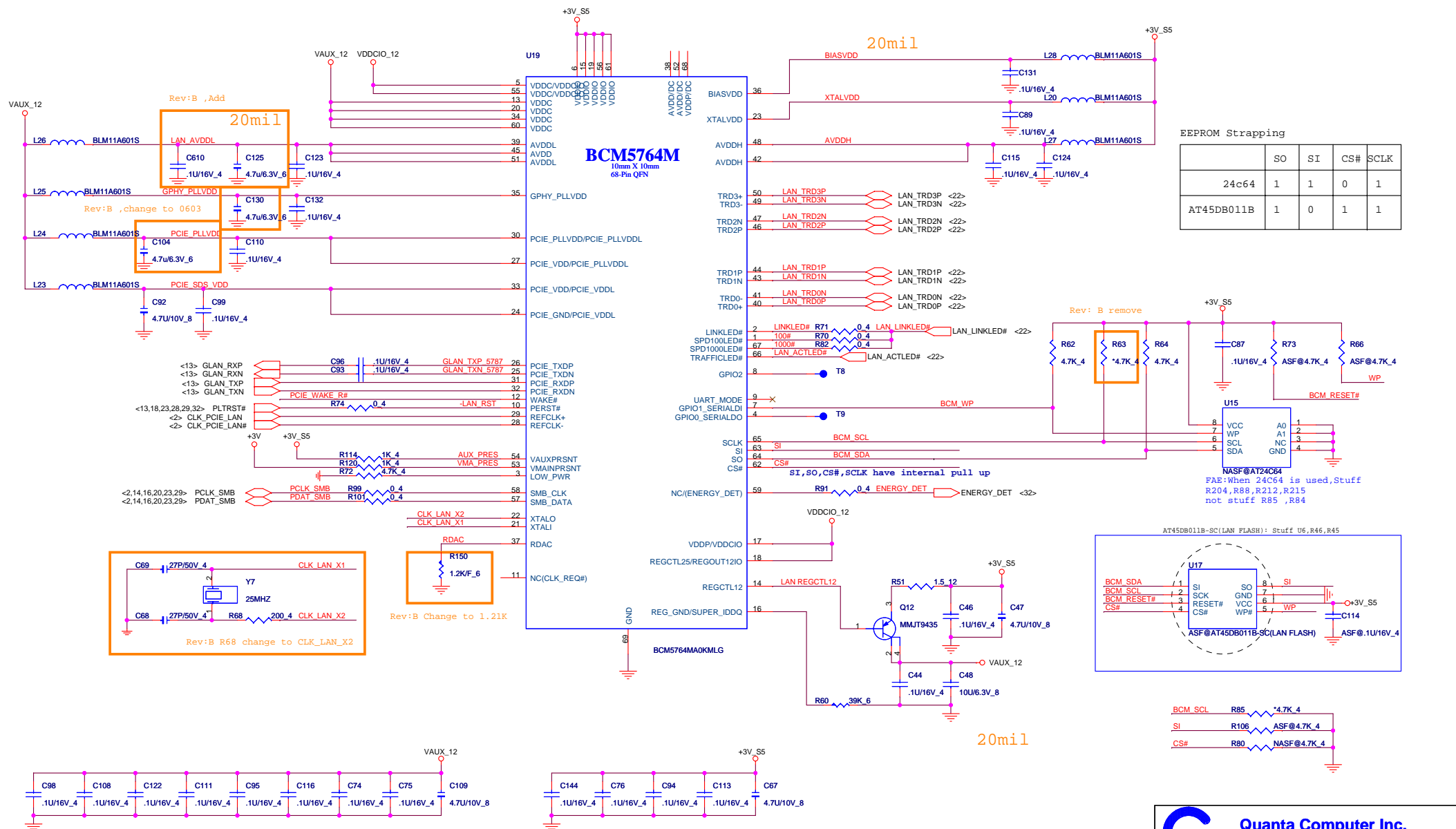
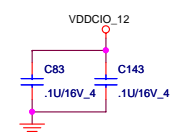
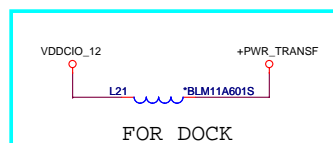
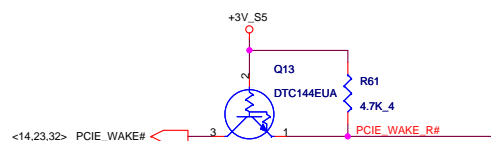




Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	LVDS/HDMI/CAMERA/LID	1A
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LAN

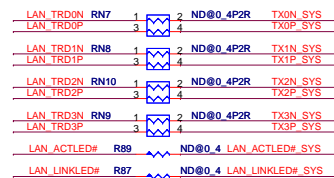
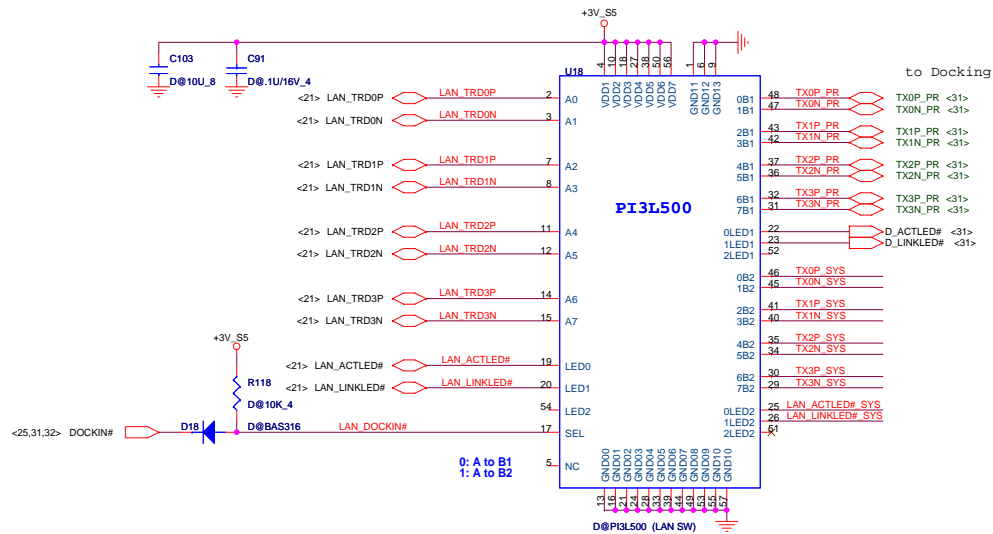


Low is normal, H->Turn Off 1.2V,
H(>0.7V <2.5V)->L will internal
reset



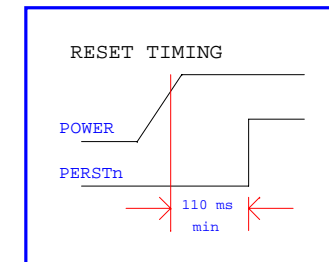
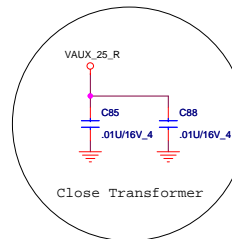
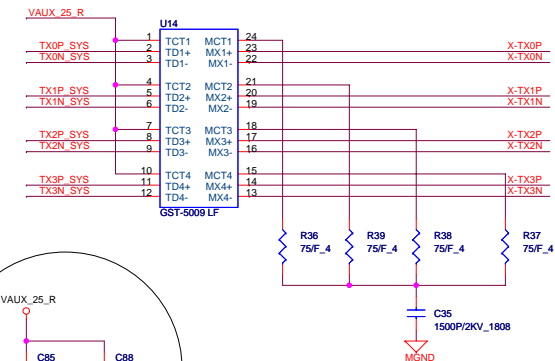
Size	Document Number	Rev
	BCM5787 & 5764 LAN	1A
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LAN SWITCH

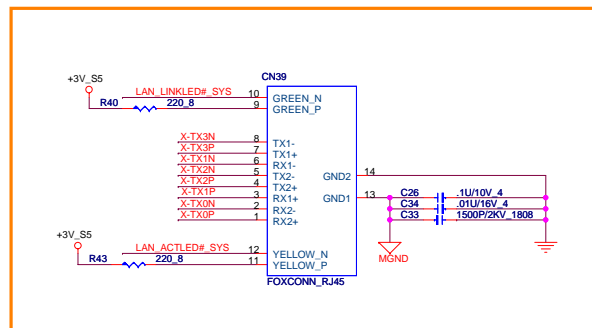


Transformer

Source 1: DELTA LFE9249 DB0ZR1LAN11
Source 2: Bothand GST5009 DBKN1NLAN03

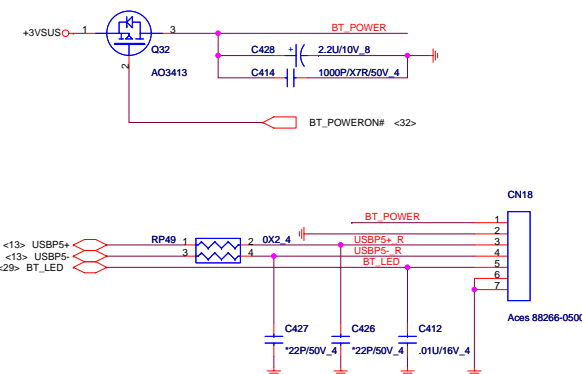


RJ45-11



9/29: change footprint
11/27: change footprint
11/28: R43 & R40 Change to 0805
1/31: Rev: C change PIN define about 9,10,11 & 12

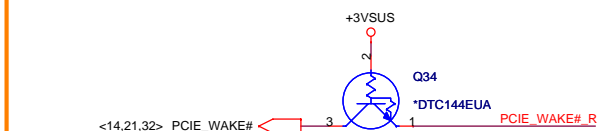
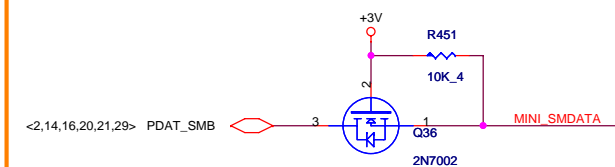
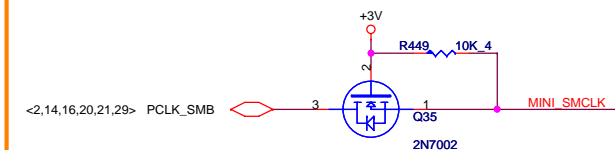
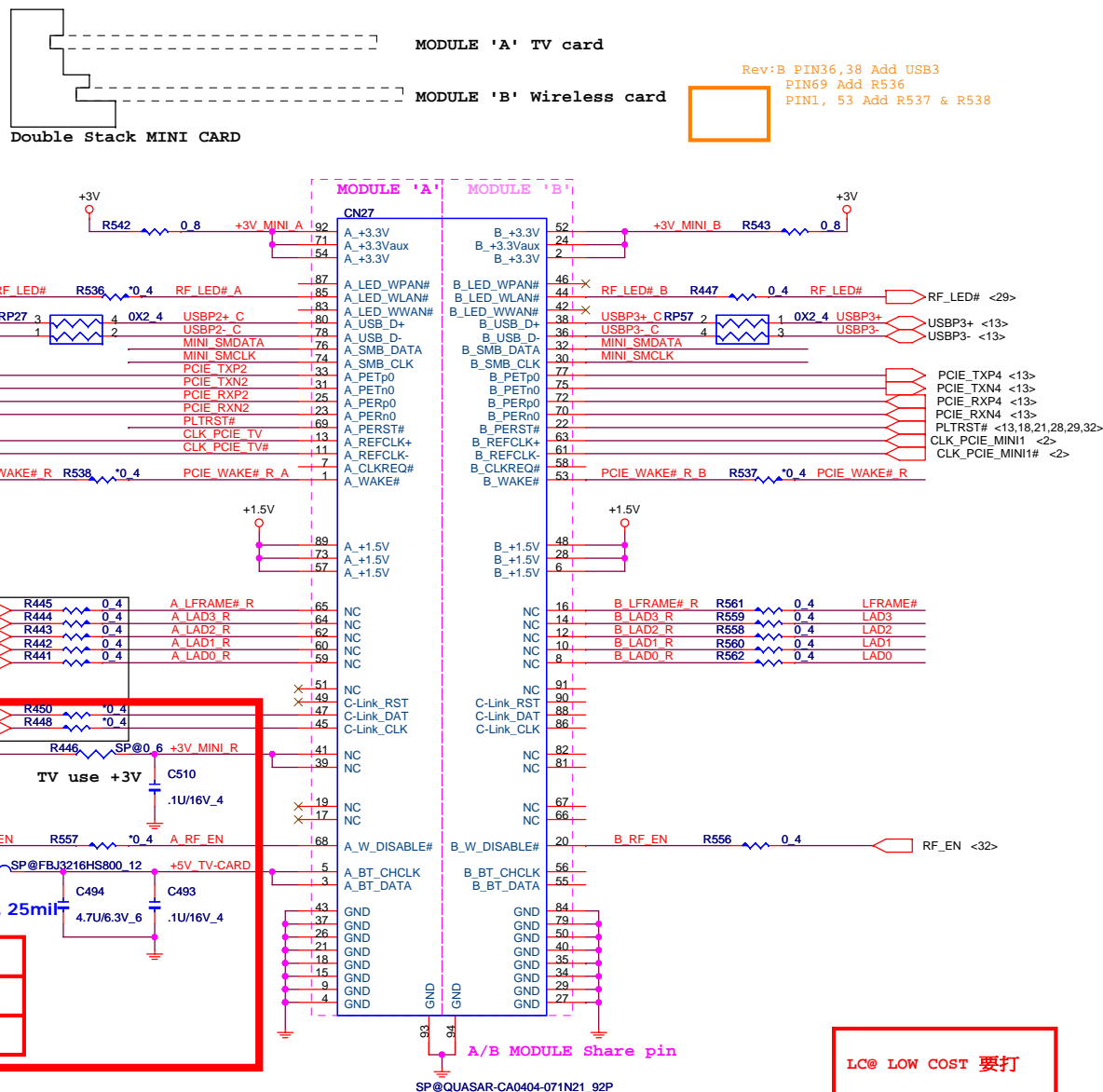
BLUETOOTH MODULE CONNECTOR



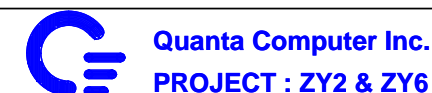
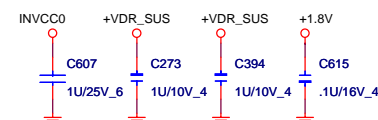
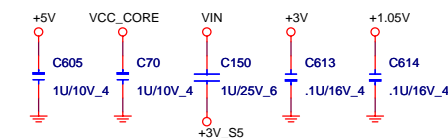
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size Document Number
BT/CCD/RJ45-11/CIR/2nd FAN
Date: Tuesday, April 08, 2008 Sheet 22 of 40 Rev 1A

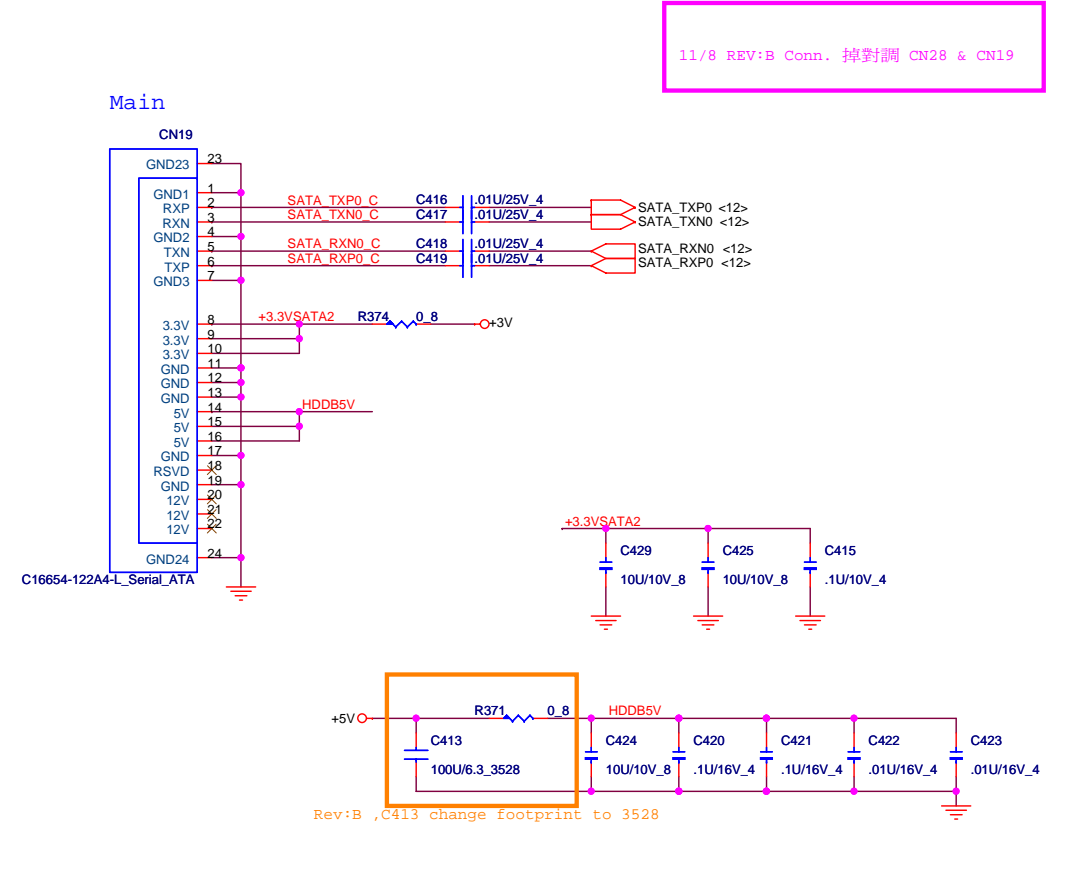
MINI-CARD



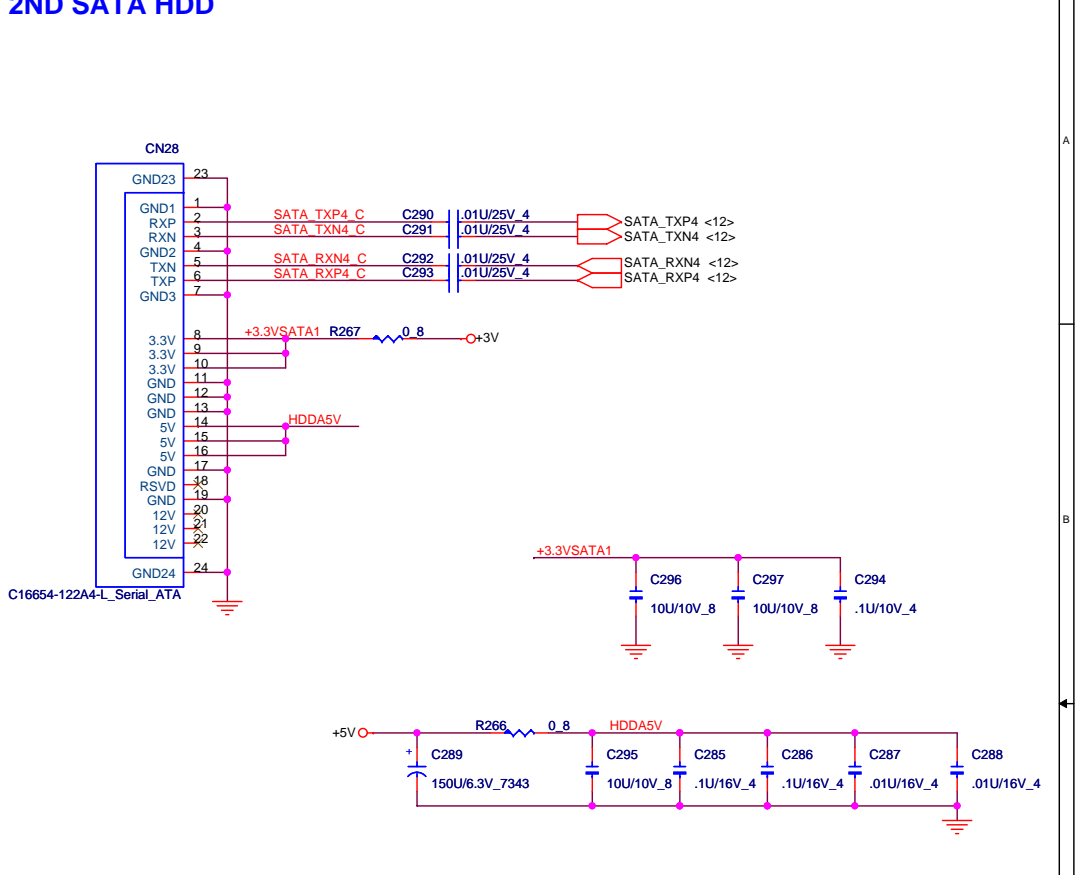
FOR EMI



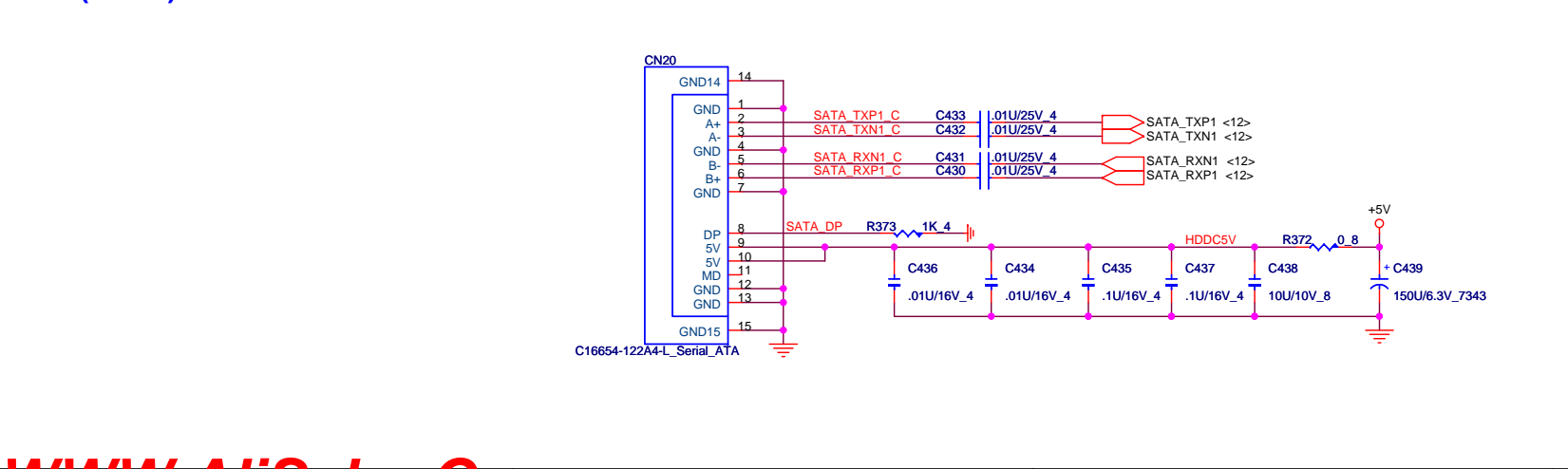
SATA HDD




2ND SATA HDD



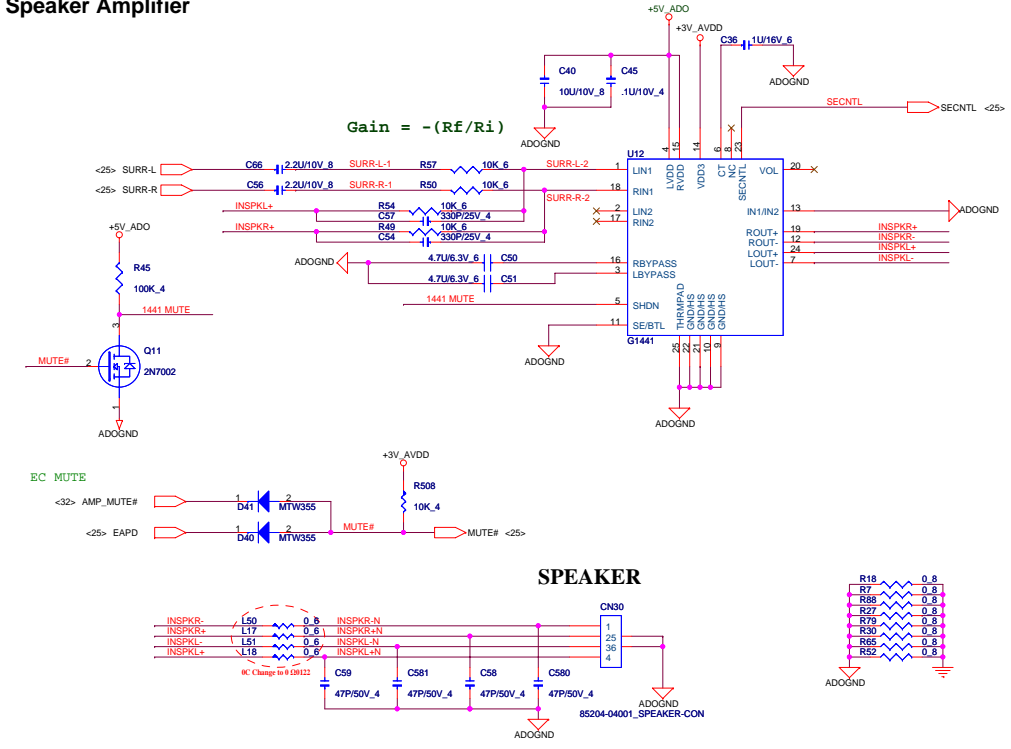
ODD (SATA)



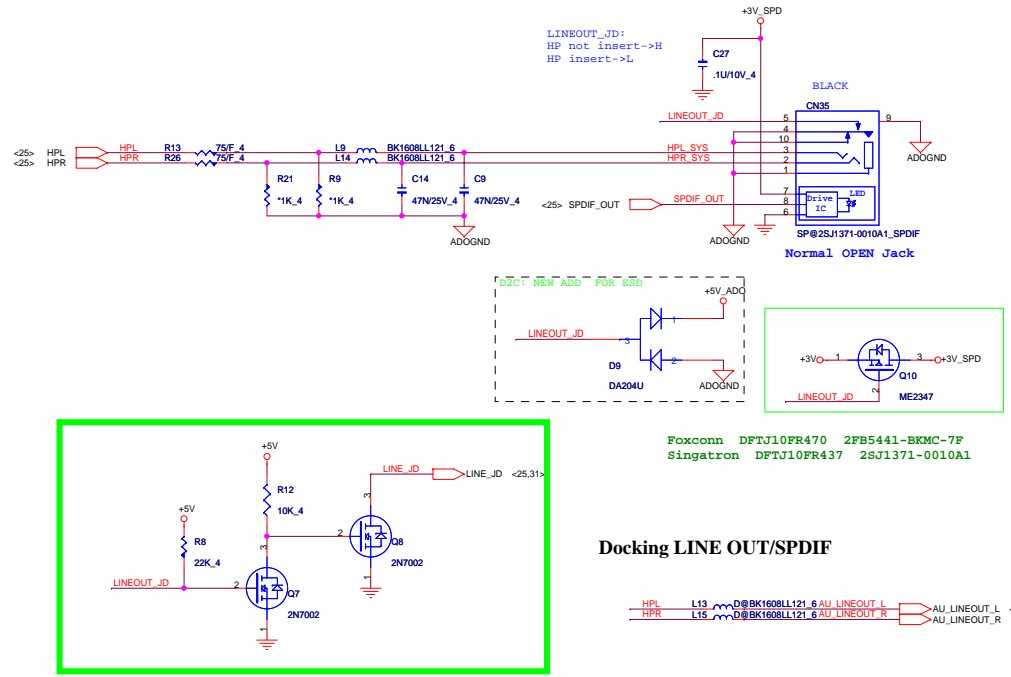
 **Quanta Computer Inc.**
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	SATA-HDD & ODD	1A
Date:	Tuesday, April 08, 2008	Sheet 24 of 40

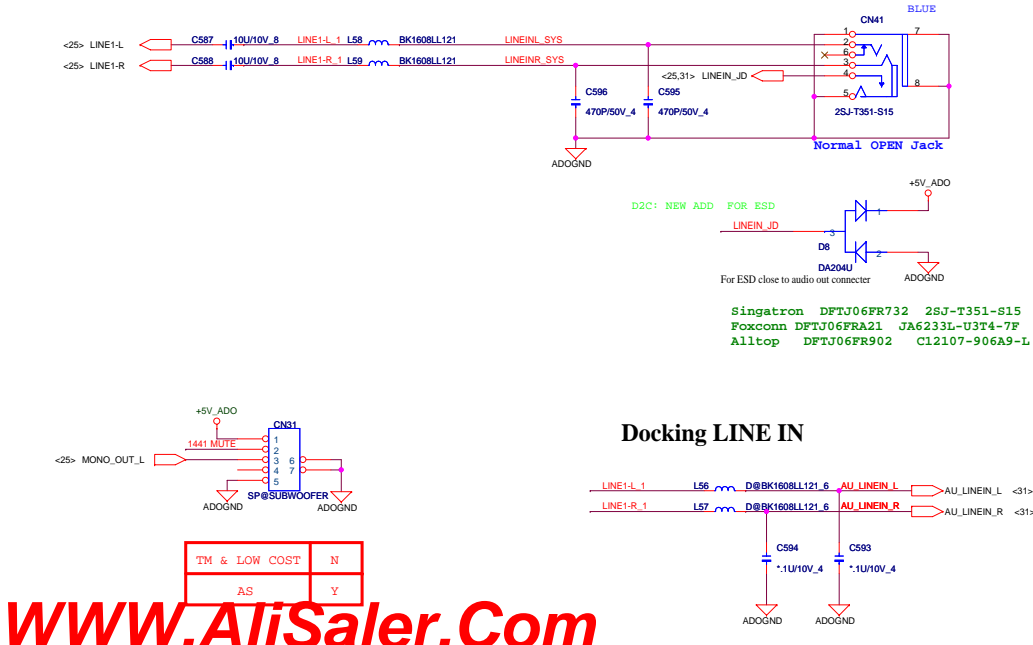
Speaker Amplifier



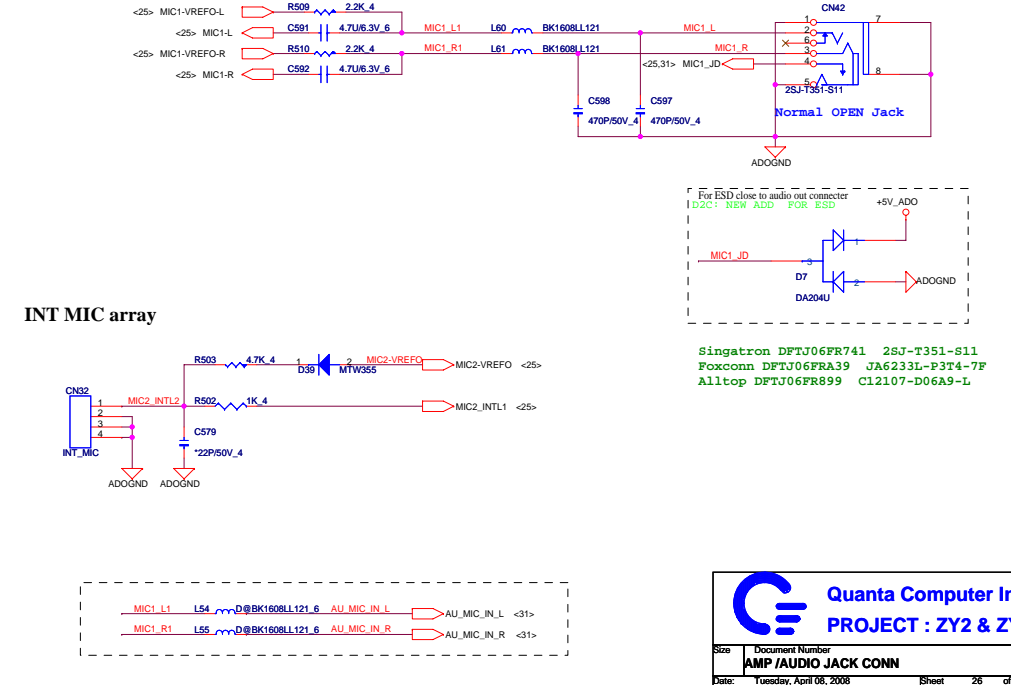
SYSTEM LINE OUT/SPDIF



SYSTEM LINE IN/SUBWOOFER



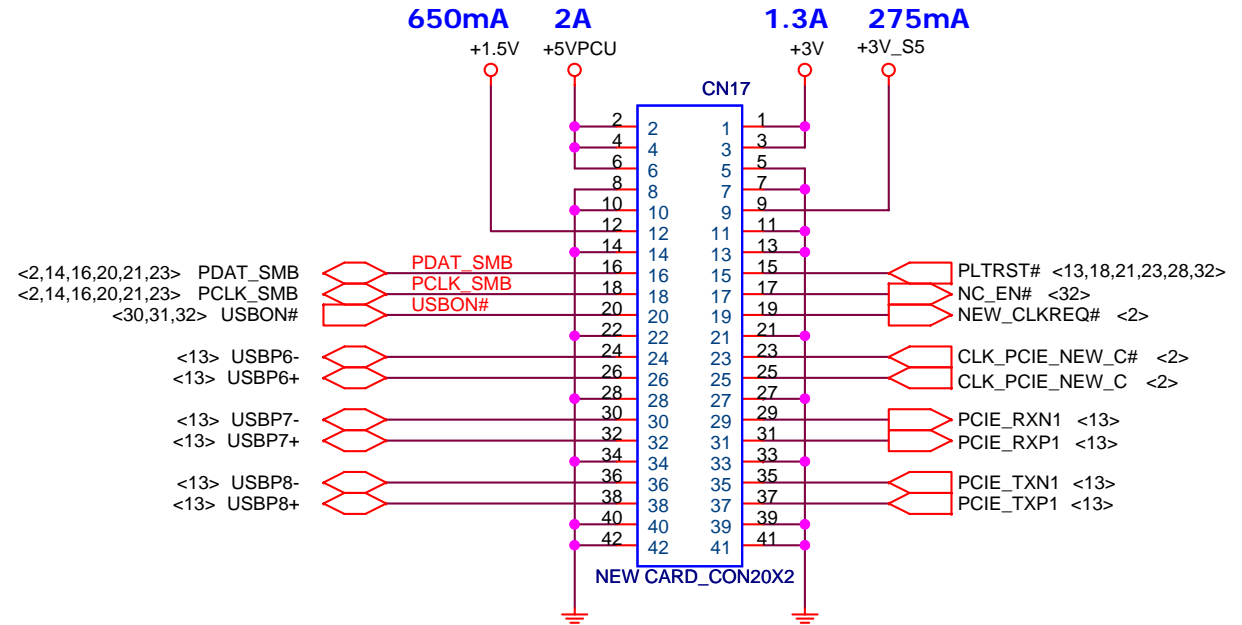
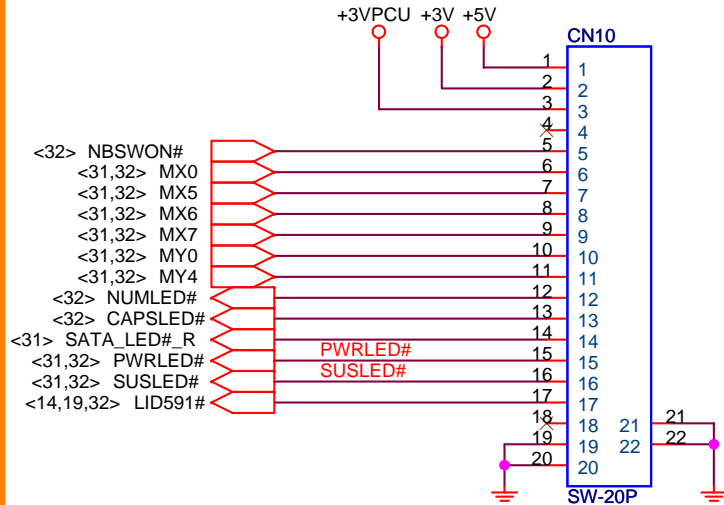
MIC



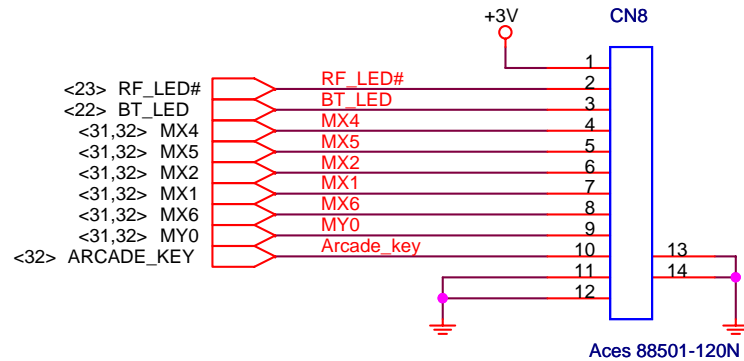
Size	Document Number PCMCIA(OZ601)	Rev 1A
Date	Tuesday, April 08, 2008	Sheet 27 of 40

To NEW-CARD & EXT. USB

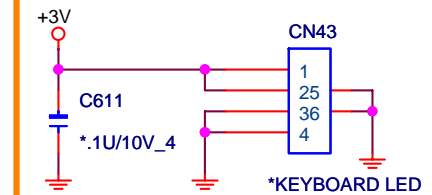
REV:B, CN10 change footprint



REV:B, Please change PIN define.same as ZY5
CN8 change footprint



Fncion	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4



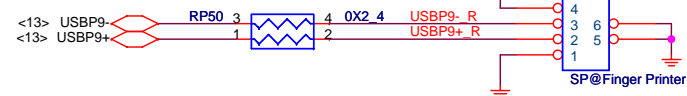
Rev:B Add CN43 For backlight KB

Rev:B Change to 圖 to 方PAD
C255,C234,C221,C199,R217,C198,R183,
R182,R174,R257,R324,R335,R334,R349,C395



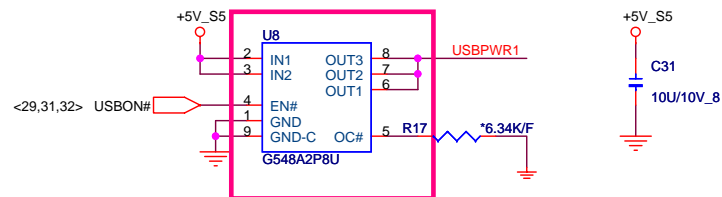
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Finger Printer

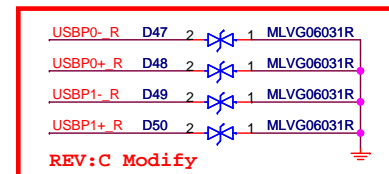


TM & AS	Y
LOW COST	N

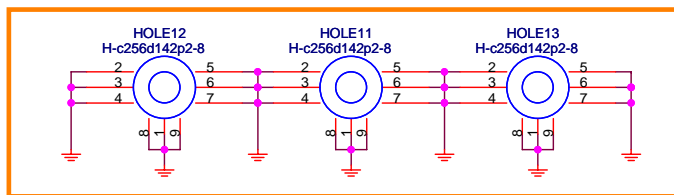
USB



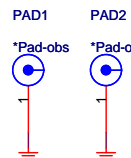
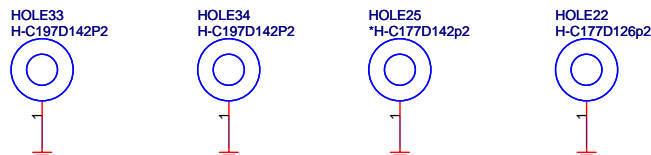
10/16: Change BOM



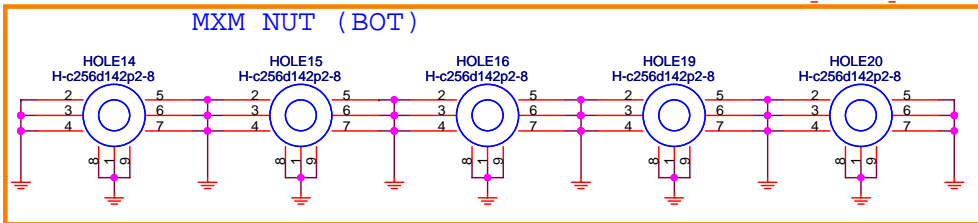
HOLES CPU NUT (BOT)



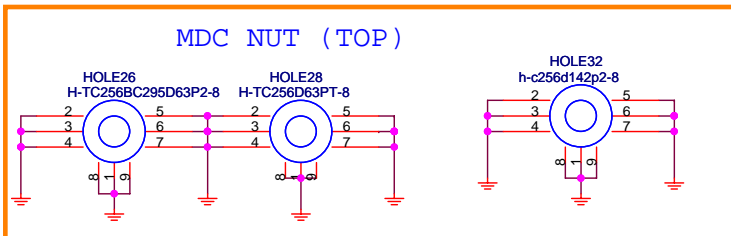
Rev : B Add MINI NUT



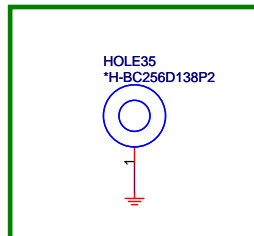
MXM NUT (BOT)



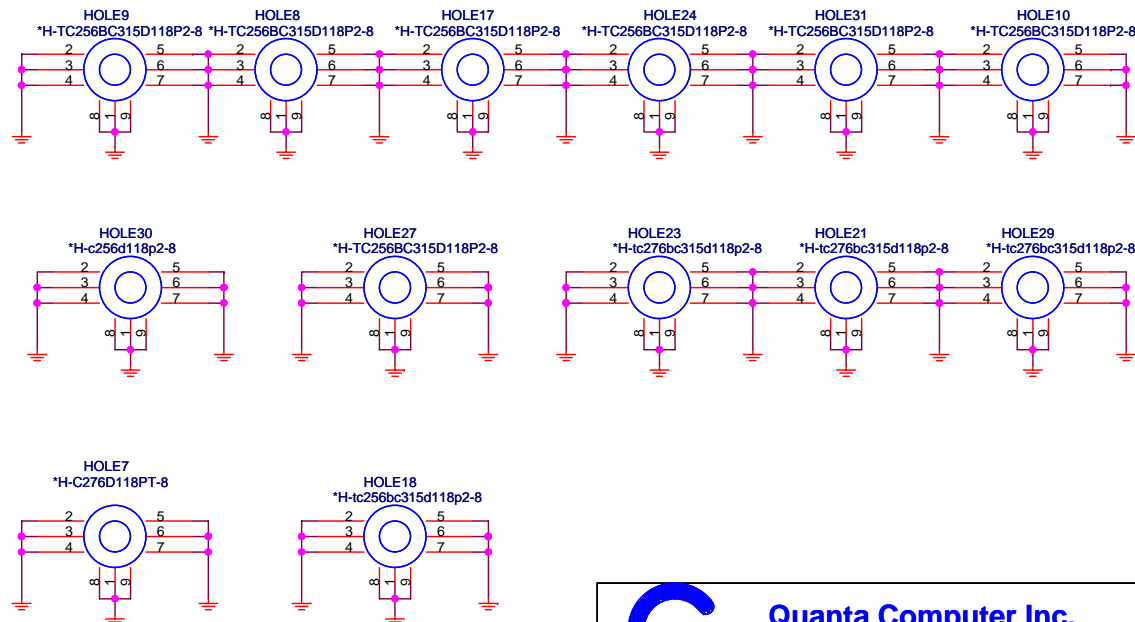
MDC NUT (TOP)



Rev:B New add HOLE32
HOLE26 & 28 Change footprint

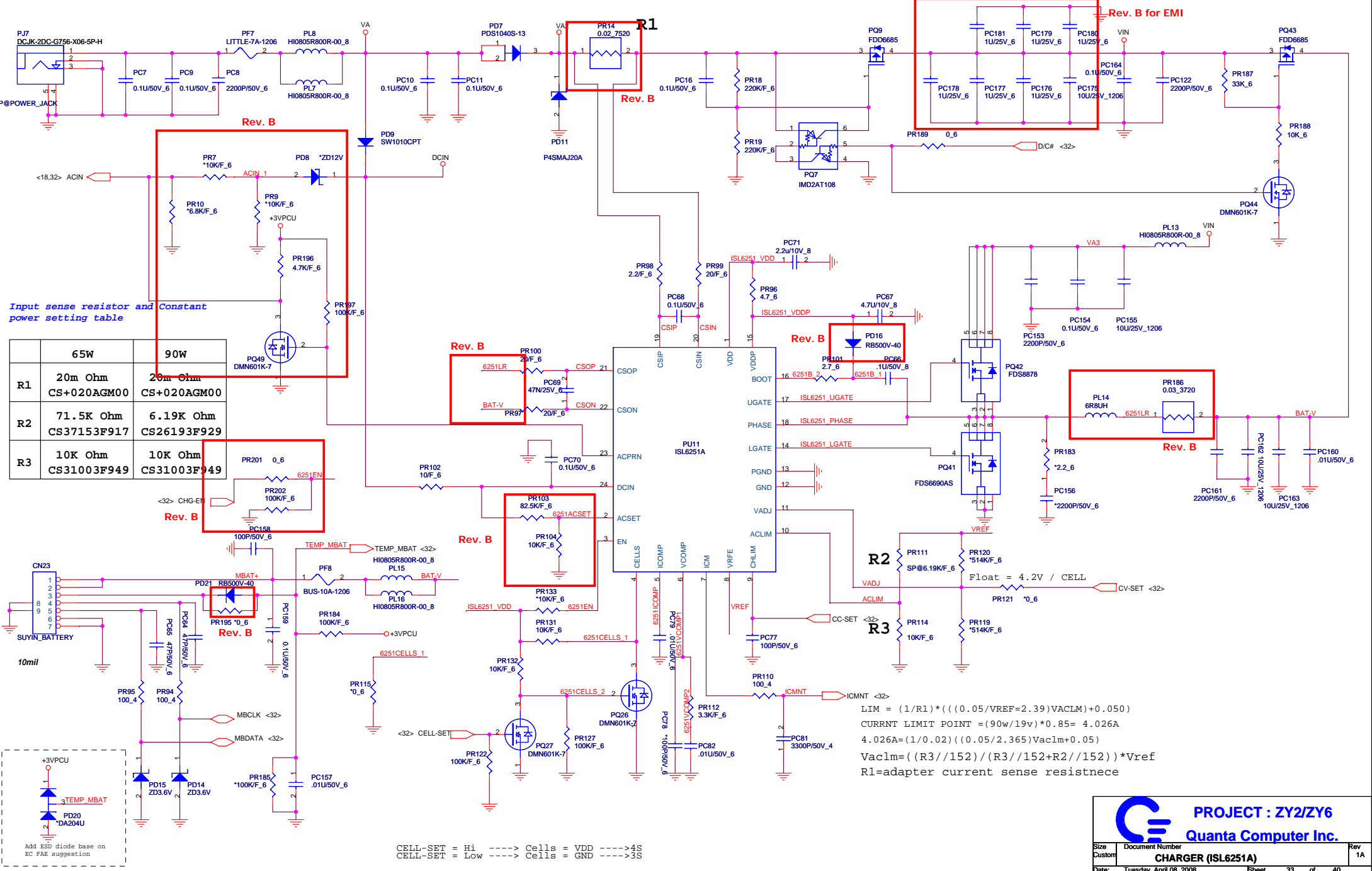


HOLE35 要搬到BOT去



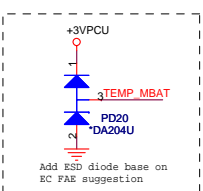
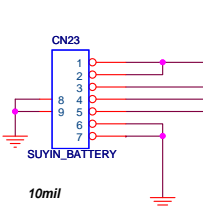
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number USB/FINGER PRINTER	Rev 1A
Date:	Wednesday, April 09, 2008	Sheet 30 of 40



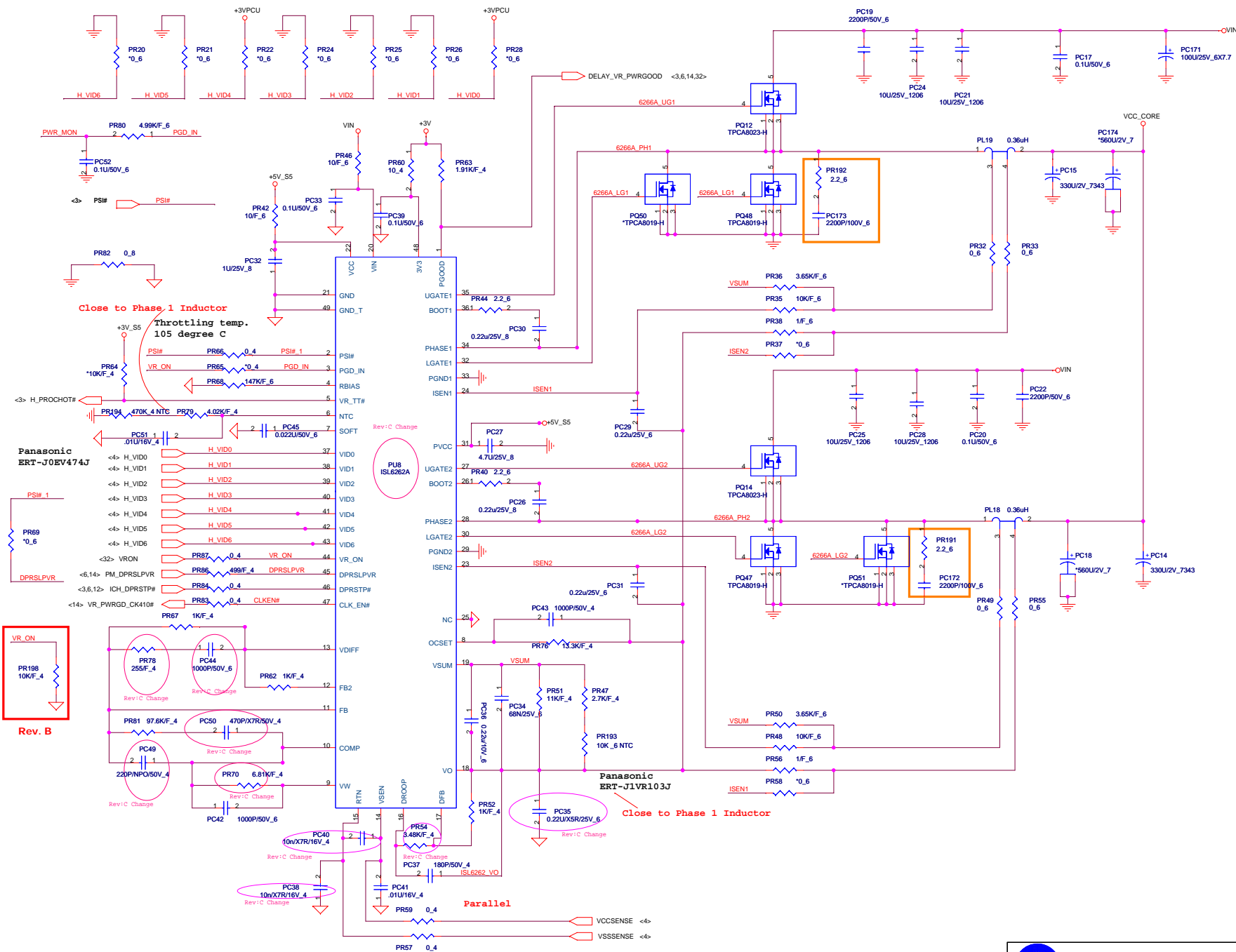
Input sense resistor and Constant power setting table

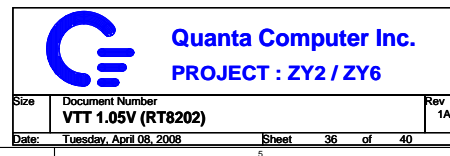
	65W	90W
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949

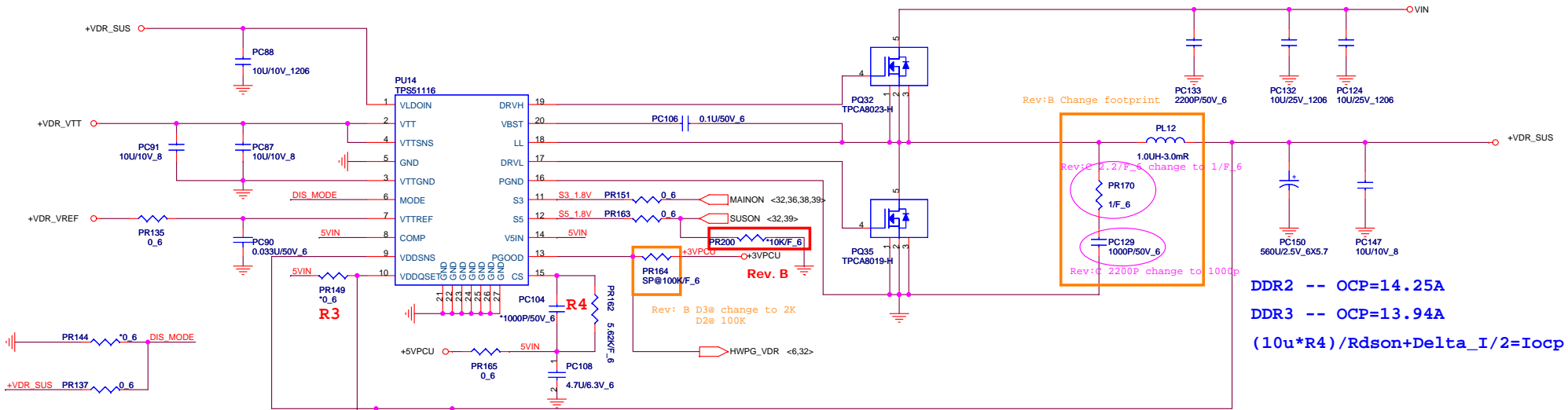


CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S

$$LIM = (1/R1)*(((0.05/VREF=2.39)VACLM)+0.050)$$
$$CURRNT LIMIT POINT = (90w/19v)*0.85 = 4.026A$$
$$4.026A = (1/0.02)*((0.05/2.365)Vac1m+0.05)$$
$$Vac1m = ((R3//152)/(R3//152+R2//152))*Vref$$
$$R1 = \text{adapter current sense resistnece}$$





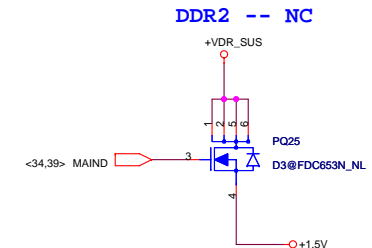
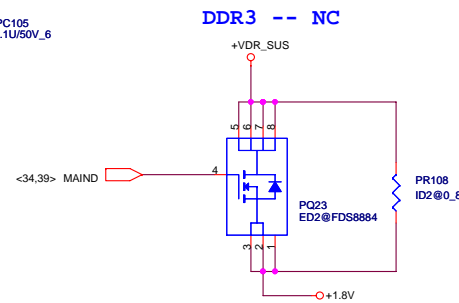


DDR2 -- OCP=14.25A
 DDR3 -- OCP=13.94A
 $(10u \cdot R4) / R_{dson} + \Delta I / 2 = I_{ocp}$

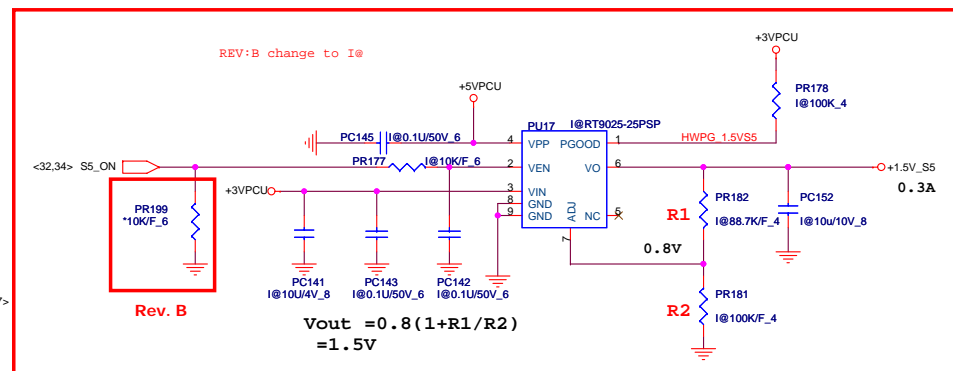
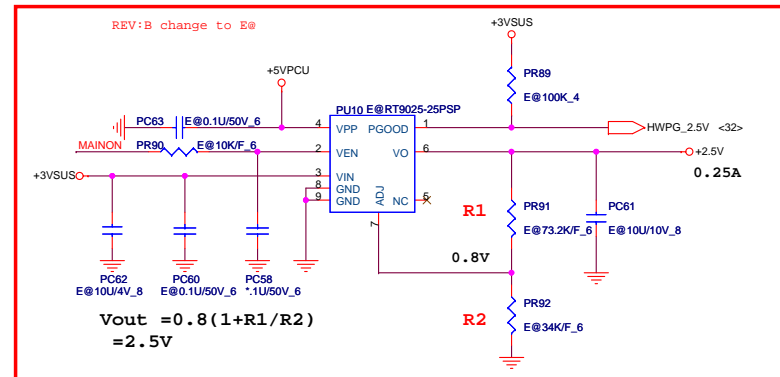
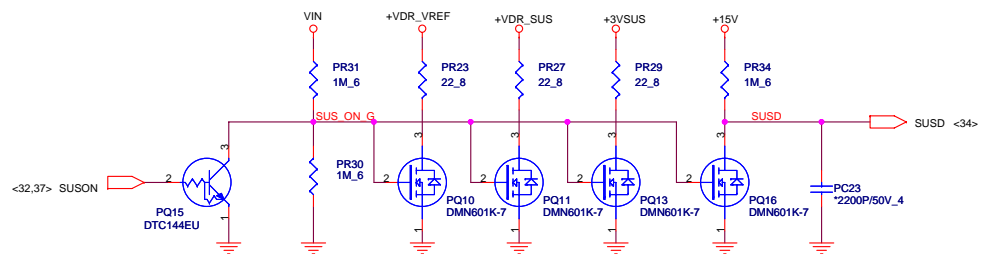
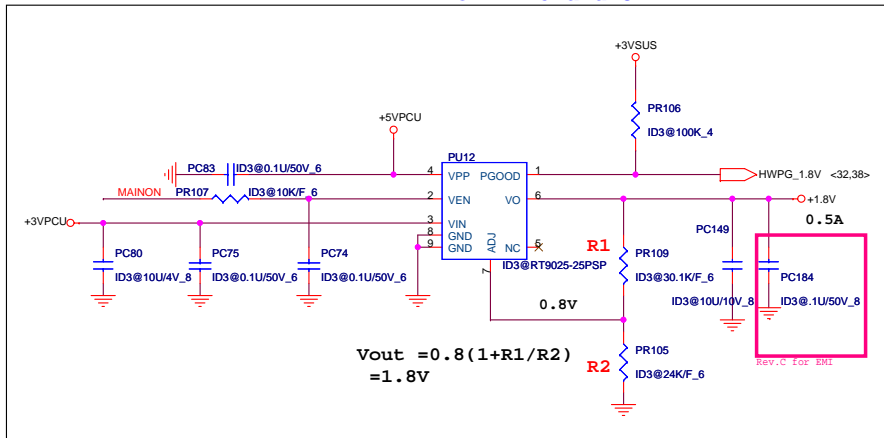
	DDR2(1.8V)	DDR3(1.5V)
R1	76.8K CS37683F927	75K CS37503F919
R2	110K CS41103F910	76.8K CS37683F927

$$R1 = (100 \cdot V_{out} - R2)K$$

if tune Vout R3 un-mount, R1 and R2 mount



for DDR3 and UMA



REV:B change to E@



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PROJECT : ZY2 / ZY6

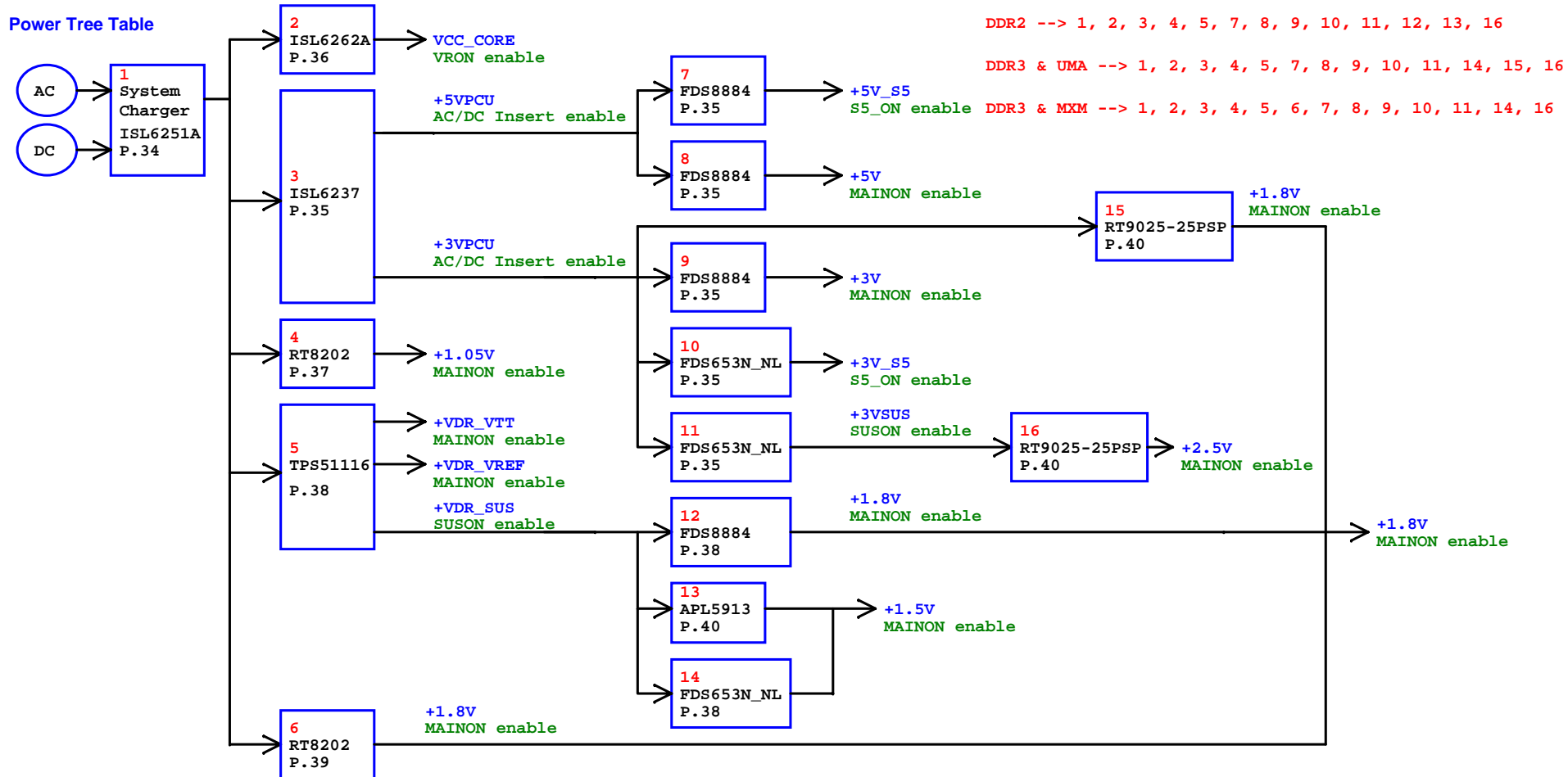
Size	Document Number Discharge (2.5V/1.5V)
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Date: Tuesday, April 08, 2008

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Rev	1A
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Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T)
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

Model	REV	CHANGE LIST	MODEL	ZY2	
				FROM	To
ZY2 MB	1A	FIRST RELEASED: E200610-3793 (PCB:)		X	1A
	1B	Page2 : Add R475 ,531 & R532 to avoid active error. (follow CK505 design guideline) Page2 : Swap SRC4 & SRC9, because NEW_CLKREQ# is only to control SRC1 or 4 Page3 : Add R540 to avoid active error. (CPU Thermal monitor) Page6 : Follow DDR3 spec R251 change to 10K. Page18 : POP C282 &C284 and RSVD. C604 for DDR3 PCB boot issue. Page18 : HDA_RST# PIN change from 151 to 134 for customer request. Page18 : Swap Net:TX0 &TX2 (RN15 & RN17) For HDMI no function issue. Page20 : Add R527 ,R528 ,R529 ,R530 ,R539 ,R148 ,R153 ,R152 ,R104 & R105 for vendor request.(HDMI level shifter) Page20 : Change HDMI SW IC (U9) & schematic Page23 : Add R536 ,R542 ,R538 ,RP57 ,R537 customer request.(MINI PCI-E card function) Page25 : add Intel Low Power ECR Solution(Audio) Page28 : Add part for D3 Enhanced (D3E).(oerd reader) Page29 : Add Keyboard LED function for customer request. Page30 : Location :C25 & C23 change to 100U & POP it for customer request.(USB) Page31 : Add D43 for customer request(FOR Dock :CRT _SENSE#) Page31 : CN12 & CN14 change footprint.(K/B & T/P CONN.) Page31 : Add C609 ,C606 & C608.(FOR DOCK : +5V & +5V_S5)		X	1A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
	2A	Page19 : change U22 LVDS PWR SW IC to TI for display issue Page21 : remove 5787 schematic Page23 : Add C605 ,C70 ,C150 ,C613 &C614 for EMI request Page23 : Change CN27 CONN. & schematic for intel WL burnout issue Page25 :change U13 packing from TQFN to TDFN for vendor request		1A	2A
	2B	Page20 : Add		1A	2A
				1A	2A
				1A	2A
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2B	3A
				2B	3A
				2B	3A
				2B	3A
				2B	3A